COMPARISON AND EVALUATION OF THE SINGLE-PHASE FIVE-LEVEL VIENNA WITH FIVE-LEVEL SMC USING SIC DEVICES IN TERMS OF ITS PERFORMANCE AND FAULT TOLERANCE

SO SÁNH, ĐÁNH GIÁ VIENNA 5 MỨC MỘT PHA VỚI SMC 5 MỨC SỬ DỤNG CÁC LINH KIỆN ĐIỆN TỬ SIC VỀ HIỆU SUẤT VÀ KHẢ NĂNG CHỊU LỖI

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Abstract:

The VIENNA converter is best known for using the fewest semiconductor devices. The purpose of this paper is to do a comparative analysis of the overall loss of the 5-level VIENNA converter, and to compare the fault tolerance of this converter with equivalent 5-level Stacked multicell converter (SMC). New SiC MOSFET and SiC JFET are used, in term of conduction losses and switching losses, SiC MOSFET is better. Both 5-level VIENNA and SMC topologies are studied in this article have fault tolerant capability. But to get that capability in the design, the SMC diodes have to choose with double of rating voltage, which also greatly increases the conduction losses. In terms of energy VIENNA is better than SMC, but in terms of fault tolerance, VIENNA allows the first short-circuit, and for the second fault, it needs to be equipped with fusible at both terminals. PSIM simulation is realized for validation this study.

Keywords:

Multilevel converter, Power losses, Short-circuit fault, Fault tolerant.

Tóm tắt:

Bộ chuyển đổi VIENNA được biết đến nhiều nhất vì sử dụng ít linh kiện bán dẫn có điều khiển nhất. Mục đích của bài báo này là thực hiện phân tích so sánh tổn thất chung của bộ chuyển đổi VIENNA 5 mức và so sánh khả năng chịu lỗi của bộ chuyển đổi này với bộ chuyển đổi SMC 5 mức tương đương về công suất. Hai loại van mới SiC MOSFET và SiC JFET được sử dụng, xét về tổn thất dẫn điện và tổn thất chuyển mạch, SiC MOSFET tốt hơn. Cả hai cấu trúc liên kết VIENNA và SMC 5 mức được nghiên cứu trong bài viết này đều có khả năng chịu lỗi. Nhưng để có được khả năng đó trong thiết kế, điôt của bộ SMC phải chọn điện áp định mức gấp đôi, điều này cũng làm tăng đáng kể tổn thất dẫn điện của mạch. Về mặt năng lượng thì VIENNA tốt hơn SMC nhưng về khả năng chịu sự cố thì VIENNA cho phép ngắn mạch thứ nhất, còn để chịu được sự cố thứ hai thì phải trang bị cầu chì ở cả 2 cực. Mô phỏng PSIM được thực hiện để củng cố nghiên cứu này.

Từ khoá:

Bộ biến đổi đa mức, tổn thất công suất, lỗi ngắn mạch, khả năng chịu lỗi.

1. INTRODUCTION

The study of the behavior of the VIENNA converter following the failure of a power switch aims to analyze the constraints generated by the fault in order to check whether the safety of the converter is ensured and whether degraded operation is possible. Based on this analysis, suitable protections are proposed and dimensioning criteria are laid down to guarantee the safety of the converter from the design stage and possibly increase the availability of the application. If the converter continues to operate under short-circuit switch conditions, the next problem may occur in other semiconductor devices or on the connected part to the DC-link. Usually, the converter will pause to review the problem and repair it. However, a sudden stop of the converter system causes significant economic losses in some application such as wind energy conversion. In a different way, modern power electronics make extensive use of MOSFETs in many applications and in the future, there will be more and more applications using MOSFETs [1]. Although the specification of MOSFETs is well documented, the practical aspects of controlling them in specific circuit configurations at different power levels and at different frequencies require designers to pay attention to several aspects. Here, the author presents the focus on the application of SiC MOSFETs for 5-level VIENNA sets and the selection of modern semiconductor devices with SiC technology in the circuit. Lower parasitic capacitance, RDS (on), RGint, Qg, Rthjc and much faster switching times are being achieved in newer MOSFETs.

The focus of the paper is to analyze and compare the fault tolerance of the 5-level VIENNA converter compared with the 5-level SMC converter including Short-circuit mode [2]. From there, select the suitable semiconductor devices for the 800VDC load, and compare the total losses of the two converters with the different SiC MOSFET, SiC JFET and diode solutions.

2. FUNDAMENTAL PRINCIPAL CONTROL STRATEGY PHASE OPPOSITE DISPOSITION (PoD)

As shown in Fig. 1, the single-phase five-level VIENNA converter composes of two active switching devices (T1, T2), two switching diodes (D1, D2), four clamped di-odes (D3, D4, D5, D6) two rectified diodes (Dp, Dn), two flying capacitors and two DC-link capacitors. Topology divides into two stacks: upper stack (corresponding to capacitors: Cf1 and Cs1) and lower stack (corresponding to capacitors: Cf2 and Cs2) [3].

The operation of topology can be expressed by five switching states, (‘Level 2’, ‘Level 1’, ‘Level 0’, ‘Level -1’ and ‘Level -2’), and their corresponding input voltage are shown in Table 2.

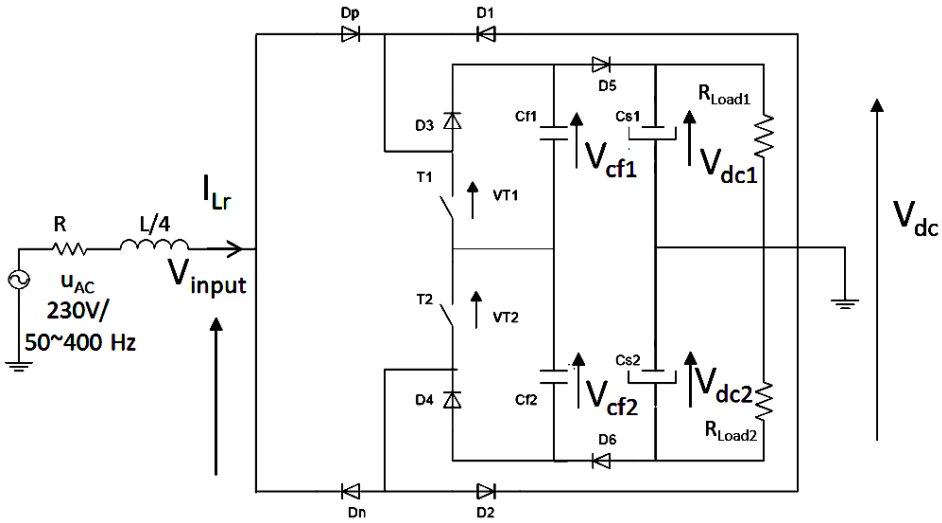


Fig. 1. Single-phase five-level VIENNA PWM converter with only two active power semicon ductor devices

Table 1. Relationship between input voltage and switching signals

Phase Voltage (V_{input})	Level	Switching Signals	
		T1	T2
Vdc/2	±2	OFF	OFF
Vdc/4	±1	OFF	ON
Vdc/4	±1	ON	OFF
0	0	ON	ON

The modulation consists in providing the input AC voltage with the minimum THD and the balancing management of the two flying capacitors. In 5-level operation, two carriers have to be used (Figure 2). This solution can be used if the natural balancing property is realized through an additional input filter tuned at the switching frequency. Here, this approach is not matching with a fault-handling strategy because the reduction of the apparent frequency in fault mode creates a resonance with the input filter that is tuned at the same frequency. A solution can be used as low frequency active balancing by controlling the different duty cycles. The features show us how the different components of the structure work. That notices the complementarity of the diodes, one diode operates on the positive alternation the other on the negative alternation, the operation is identical to that of the 3-level, the transistors as for them operate on the totality of the alternation. The V_{cf1} oscillates on the positive alternation and V_{cf2} on the negative alternation, the floating voltage is connected to the output bus by clamp diodes, the ripple is done according to the state of charge of the floating capacitors (Figure 3). On the positive alternation V_{cf1} (symmetrical operation V_{cf2}). If $V_{cf1}+V_{cf2} > V_{dc}/2$ the clamp diode D_5 is on discharge of C_f. If $V_{cf1}+V_{cf2} < V_{dc}/2$ the clamp diode D_5 is blocked charging of C_{f1}.

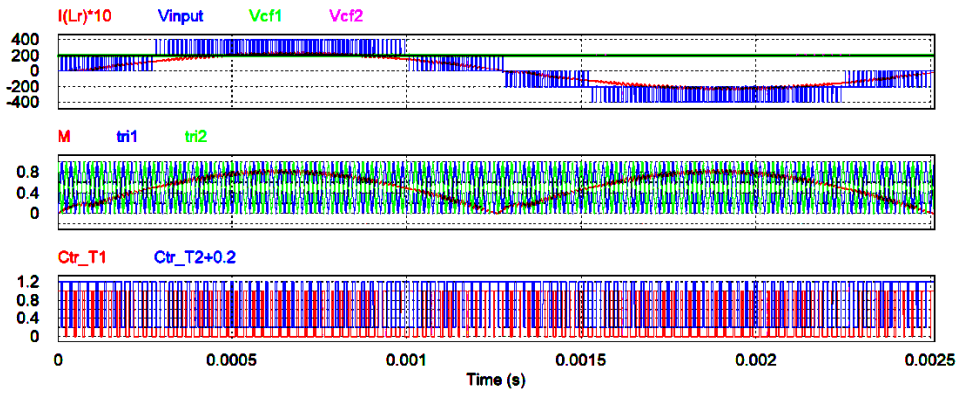


Fig 2. Fundamental control strategy POD for 5-level VIENNA Converter

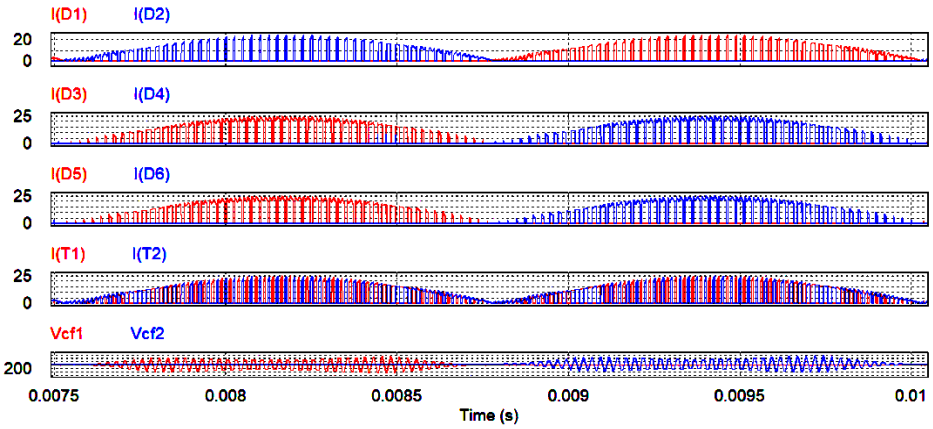


Fig 3. Currents and flying- capacitor voltages of 5-level VIENNA with (f_{AC}= 400 Hz, V_{DC}= 800 V)

3. FAULT TOLERANT CAPACITY OF 5-LEVEL VIENNA TOPOLOGY IN COMPARISON WITH 5-LEVEL SMC TOPOLOGY

3.1. Cause of fault formation in MOSFET device

In a situation of physical failure of a diode, all of the energy initially stored in the flying capacitor is released in the transistor MOSFET of the same cell. Thanks to voltage splitting, the capacitor is calibrated to half the bus voltage, so energy dissipated per component is low. Other my study of the MOSFET stresses show that no opening of the bonding can appear. The Figure 4 shows that there is a metal bridge between the source and the drain to establish short-circuit mode.

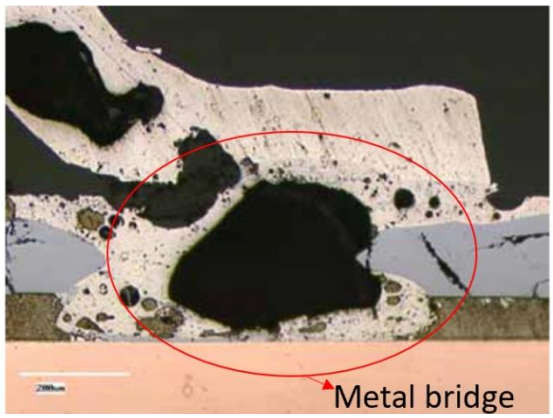
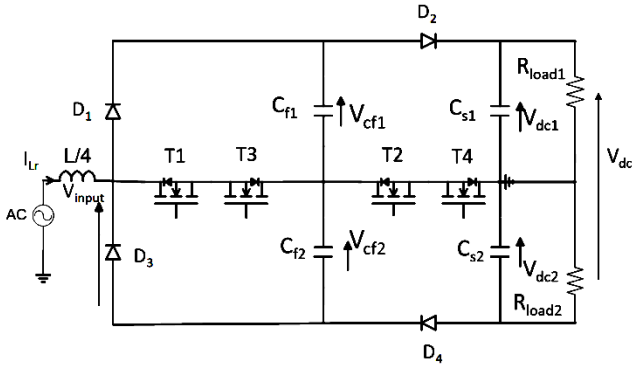


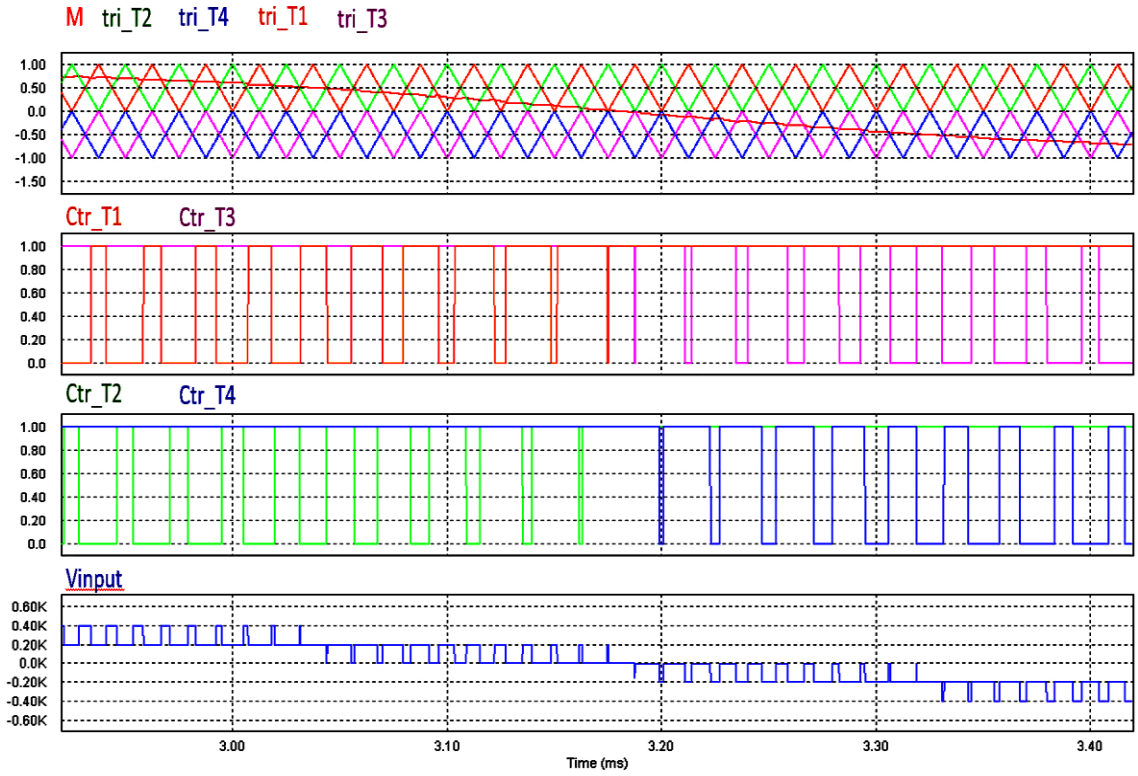
Fig 4. MOSFET destructive test (plastic-epoxy housing) in a short-circuit stress (peak-power stress)

3.2. Faulty sign of 5-level VIENNA converter in comparison with 5-level SMC con-verter

Both structures, 5-level VIENNA and 5-level SMC (Figure 5a and b) have the fault capability. The author studies the characteristics of two converters when a short-circuit fault occurs and considers the fault tolerance of the two converters. The first short-circuit failure of a transistor imposes a permanent off-state of the diode for the same cell, up to the complete discharge with a low voltage dynamic of the fly-cap towards the AC source and the DC source. One cell among four imbricated cells is failed and the topology naturally evolves from 5-level to a symmetric 3-level for VIENNA converter but an asymmetric 4-level operation for SMC converter. A second short-circuit failure of a transistor provides the short-circuit of the network through the input inductance and has to be managed by a fuse at the center- tap of the DC bus to impose a simple rectifier mode in post-failure operation. If a safe-stopping is preferred, a simple breaker can be introduced at the input. Note that, in all cases, the DC bus where typically a high energy is stored, is isolated through the reverse diodes: this is a very important and interesting safety property. On the other hand, the first short-circuit failure of a diode induces a direct short-circuit of the transistor across the fly-cap and a fast discharge appears but without risk of explosion or open-circuit of wire-bonds because the energy is low. For example, as shown in Figure 6 the operating point AC 16ARMS, 220VRMS and Fswitching (fsw) = 40 kHz, gives a capacitor value equal to 40µF at 0,8J/200V, while the energy absorption capability of a 600 V MOSFET chip (size 0,68 cm² × 165 µm) was assessed to 3J in adiabatic thermal mode [5]. Here again, the topology naturally evolves from 5-level to 3-level for VIENNA topology [6] but 4-level for 5-level SMC topology. A second on-state failure of a diode provides the second short-circuit of the transistor. This last has to be turned off through a Vdssat monitoring to avoid the short-circuit of the DC bus. Then, a simple rectifier mode can be obtained thanks to the input rectifier diode of the topology.



a)



b)

Fig 5. Single-phase five-level SMC PWM converter with four active power semicon-ductor devices [4]: a) Diagram; b) Fundamental control strategy POD for 5-level SMC Converter

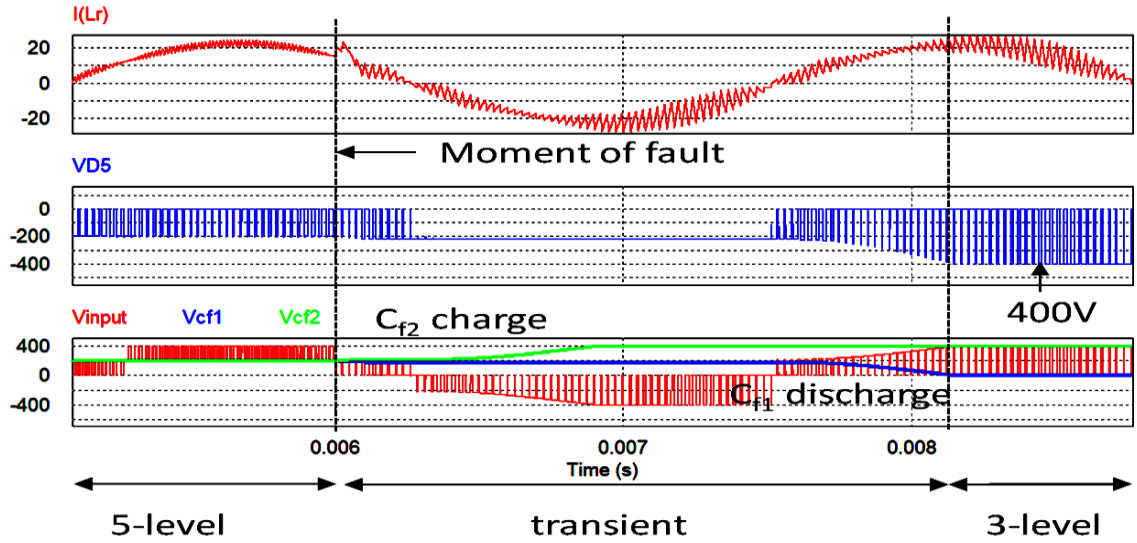


Fig 6. 5-level VIENNA with the first short-circuit
(f_{AC}= 400 Hz, U_{AC}=230 V, V_{dc} =800 V, Rf=0.1 Ω, fsw= 40 kHz)

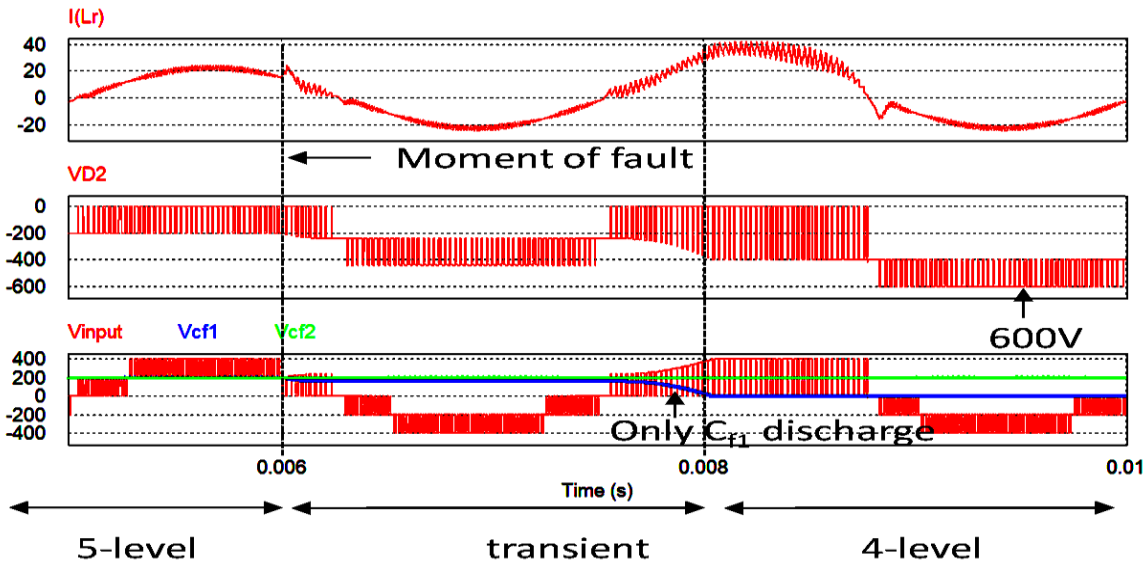


Fig 7. 5-level SMC with the first short-circuit (f_{AC}= 400 Hz, U_{AC}=230 V, V_{dc}=800 V, Rf=0.1 Ω, fsw= 40 kHz)

According this first approach, the author can conclude that a high safety is gained with theses two topologies and the proposed rating. However, concerning voltage stress after a failure, a difference exists between the VIENNA and the SMC topology. Indeed, in Figure 6 and 7, simulations show the consequence of a permanent short-circuit failure state applied to one transistor. A low dynamic discharge voltage appears identically for the two structures. However, the peak voltage across a diode of the non-failed cell differentiates the two structures: $V_{dc}/2$ = 400V for the VIENNA converter (Fig. 6) against $3V_{dc}$ /4 = 600V for the SMC converter (Fig. 7). For the first, a 600V rating is sufficient while for the second case, a 1.2kV rating is mandatory.

iV. EVALUATION OF GLOBAL POWER LOSSES OF 5-LEVEL VIENNA

The author selected the high switching semiconductor devices JFET, MOSFET and found that the SiC MOSFET has the smallest Rdson (Table2) so the calculation of converter's conduction losses will achieve the smallest losses.

Table 2. Principal parameters of semiconductor devices

Semiconductor devices	Rdson (mΩ)	Vd (V)	Rd (mΩ)
JFET SiC **UJ3N065080K3S** 650V/24A @ 100°C	80		
MOSFET SiC **C3M0045065J1** 600V/41A @ 100°C	60	1.5	200
Diode SiC **IDT16S60C (Infineon)** 600V/16A		0.825	62.5

Diode Rec **20ETS08** 800V/20A		1.07	7
Diode SiC **IDH15S120** 1200V/15A		1	114

The main focus in modern power electronics is to reduce total loss in devices and systems to achieve higher operational efficiency and more compact designs, reducing the mass and weight of the systems. Therefore, operation at higher switching frequencies is a necessity, and as a result, switching losses dominate the power dissipation in semiconductor switching. Reducing switching losses becomes the important goal.

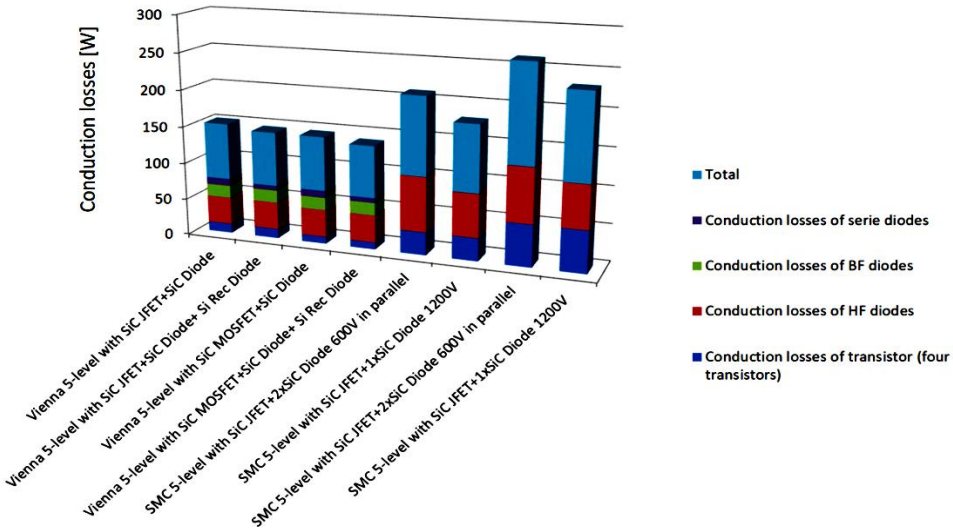


Fig. 8 Comparison of the conduction losses of the two converters corresponding to different semiconductor device selection solutions (IRMS= 16A; V_{dc} = 800V)

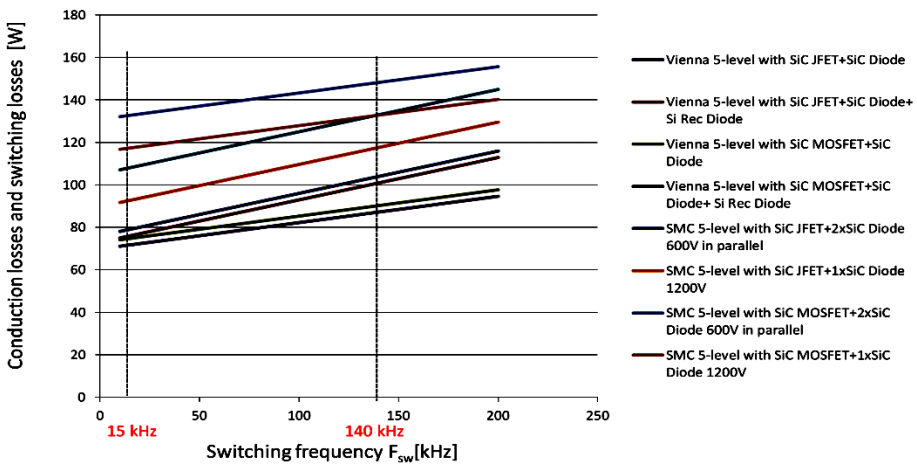


Fig. 9 Comparison of the total losses of the two converters corresponding to different semiconductor device selection solutions (IRMS= 16A; V_{dc} = 800V)

Fig. 8 presents only the conduction losses estimation and comparison including SiC MOSFET, SiC JFET and several diode type. The calculations are based on analytical average model without taking into account the current ripple on additional ohmic losses. Indeed, in first approach, if the stray inductor in different cells is not considered, two structures have the same total Volts x Amps switched and then identical switching losses for the same type of active device. Note that these last losses are low compared to the conduction losses due to using fast transistors and SiC diodes with a very low reverse recovery. Figure 9 shows the global losses including conduction and switching losses, in terms of global losses, the 5-level VIENNA converter has the advantage compare to the 5-level SMC converter. For the 5-level VIENNA, minimum loss when choosing a MOSFET device, high frequency diodes use SiC diodes and low frequency diodes use rectifier diodes. For the 5-level SMC, minimum loss when choosing a JFET device, high frequency diodes use 1200V SiC diodes instead of using 2x600V SiC diodes in series, and at high frequencies above 140k Hz, it is more advantageous to use SiC MOSFET device.

5. CONCLUSION

For critical applications, fault-tolerant converters would be the first choice. Here, the author analyzes the fault tolerance of the 5-level VIENNA converter and compares it with the 5-level SMC with the same power. The analysis shows that the 5-level VIENNA converter uses only 2 active semiconductor devices while the 5-level SMC has to use 4 active semiconductor devices. At fault mode, the 5-level VIENNA converter work at 3-level mode while the SMC work at 4-level, however the SMC must select diodes at twice rating voltage. From there, the author compares the total losses of the two converters with different options for selecting semiconductor devices to satisfy fault tolerance. The results show that the 5-level VIENNA scheme has a smaller total loss, and in most cases SiC MOSFET is a better choice than SiC JFET, especially at high frequencies.

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