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A LOW POWER, LOW NOISE CHOPPER INSTRUMENTATION AMPLIFIER USING BODY CONTROL DC-SERVO LOOP AND LOW INPUT CAPACITANCE

BỘ KHUẾCH ĐẠI CHOPPER CÔNG SUẤT THẤP, NHIỄU THẤP SỬ DỤNG VÒNG LẶP DC SERVO VÀ TỤ ĐIỆN ĐẦU VÀO NHỎ

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ABSTRACT

This paper presents a proposed low power, low noise capacitively-coupled chopper instrumentation amplifier (CCIA) using body control DC servo loop and low input capacitance applied for biomedical recording. A DC servo loop using body control (DSL-BC) is proposed to reduce the electrode offset and its noise contribution. A T-bridge capacitance network is employed in the negative feedback loop to save the chip area. Also, a positive feedback loop (PFL) is utilized to improve input impedance. The proposed circuit is simulated in a standard 0.18µm CMOS technology. According to simulated results, the proposed CCIA achieves the closed-loop gain of 40dB and the input-referred noise of 2.4µVrms over a bandwidth from 1 to 200Hz. The noise efficiency factor NEF of 6.6 is obtained while drawing current consumption of 1µA from a 1V supply. The active chip area occupies only 0.083mm^2.

Keywords: *CCIA, capacitively-coupled chopper instrumentation amplifier, DC servo loop.*

TÓM TẮT

Bài báo trình bày một đề xuất bộ khuếch đại chopper công suất thấp, nhiễu thấp sử dụng vòng lặp DC servo và tụ điện đầu vào nhỏ ứng dụng trong y sinh. Một bộ DC servo sử dụng điện áp điều khiển cực bulk của cặp transistor đầu vào của G_{m1} được đề xuất để làm giảm không chỉ electrode offset mà còn giảm sự đóng góp nhiễu của nó. Một mạng T-bridge tụ điện được dùng trong vòng lặp ngược để tiết kiệm được diện tích chip. Hơn nữa, một vòng lặp tích cực được dùng để cải thiện trở kháng đầu vào. Bộ đề xuất được mô phỏng trên công nghệ CMOS 0,18µm. Theo như kết quả mô phỏng, bộ đề xuất CCIA đạt được hệ số khuếch đại 40dB, input referred noise là 2,4µVrms qua băng thông từ 1 đến 200Hz. Hệ số hiệu quả tiếng ồn NEF là 6,6 trong khi công suất tiêu thụ dòng điện là 1µA từ điện áp nguồn 1V. Diện tích của bộ khuếch chopper chỉ chiếm 0,083mm^2.

Từ khóa: *CCIA, bộ khuếch đại chopper, vòng lặp DC servo.*

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1. INTRODUCTION

The neural signals such as electroencephalogram (EEG) and electrocardiogram (ECG), which are from the brain and the heart, are used not only for clinical purposes but also in the brain-computer interfaces (BCIs) [1]. The amplitude of bio-potential signals is pretty small, around 1mV for ECG and 10 to 100µV for EEG. These signals occupy a frequency range of from 0.5 to 150Hz [2]. The recording system often includes an instrumentation amplifier (IA) to amplify the low amplitude neural signals before processing. Nowadays, CMOS technology has been developing very strongly, and it helps electronic devices to be shrink. However, most previous works [3-5] occupy a large chip area caused by using the large input capacitor. Thus, this issue is to be limited to multi-channel recording applications. The electrode-tissue interface normally generates the electrode offset voltage V_{EOS} [6], which can be up to 50mV due to the electrochemical effects. Hence, V_{EOS} can be to saturate the amplifier.

In this work, we introduce a DC servo loop using body control for reducing its noise contribution during blocking the electrode offset. Besides, the T-bridge network capacitance is applied to the negative feedback loop. Hence, the input capacitance can be reduced, leading to saving chip area and improving the input impedance.

2. AMPLIFIER ARCHITECURE

The schematic of the proposed CCIA using body control DSL (DSL-BC) is shown in Fig. 1. The main path of CCIA comprises a two-stage amplifier to achieve high DC gain [7, 8]. The input stage, labeled G_{m1}, employs a folded cascode (FC) amplifier, while the output stage, G_{m2}, utilizes a common source (CS) amplifier to achieve a rail to rail output swing. The Miller capacitors $C_{m1,2}$ are added to G_{m2} for the amplifier stability. At 1V supply, the current consumption of G_{m1}, including its common-mode feedback (CMFB), and G_{m2} is 800 and 180nA, respectively. The proposed CCIA uses three feedback loops to define a

closed-loop gain, realize electrode offset removal, and improve the input impedance.

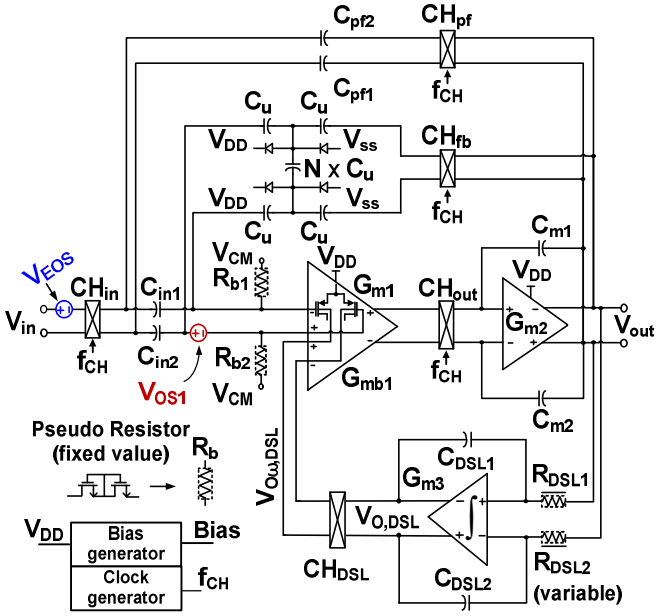


Figure 1. Schematic of the proposed CCIA using body control-DSL

As shown in Fig. 1, the DSL is used to realize a connection from the output to G_{m1}. The DSL is employed to filter out and amplifies output offset. The DSL's output voltage ($V_{O,DSL}$) is converted to $V_{O\omega,DSL}$ by chopper CH_{DSL}. As we know, the body, such as a second gate, can control the current through the channel [9]. Thus, a proposed DSL uses the differential input CMOS transistors' body instead of the capacitance C_{dsl} [10] to prevent V_{EOS}. The op-amp in the DSL-BC consumes 30nA from the supply voltage of 1V. When DSL-BC is enabled, the high pass corner is calculated as:

$$f_{hp} = \eta \frac{C_{in}}{C_{fbeq}} f_{ugb} \quad (1)$$

where $\eta = g_{mb1}/g_{m1}$ with g_{mb1} and g_{m1} are the transconductance of the buck and gate of the input pair CMOS transistors of the input stage. $f_{ugb} = 1/(2\pi R_{DSL}C_{DSL})$ is the unity gain frequency of the DSL's integrator.

Because the closed-loop gain A_V of the amplifier is defined by the ratio of the input and negative feedback capacitances C_{in}/C_{fb}. To obtain a large A_V, either the feedback capacitance C_{fb} must be reduced, or the input capacitance C_{in} has to increase. Increasing input capacitance C_{in} leads to reduce the input impedance Z_{in} and increase the chip area while reducing the negative feedback capacitance C_{fb} is restricted by the mismatch, parasitic capacitance and the constraint of the process technology [11]. Thus, the T-bridge capacitance network [11] is utilized in this work. The closed-loop gain of the amplifier can be rewritten as:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{C_{in}}{C_{fbeq}} = \frac{M \times C_U}{C_U/2(N+1)} = 2M(N+1) \quad (2)$$

In this work, C_U = 200fF, C_{in} = M x C_U = 10 x 200fF = 2pF and N = 4. Therefore, the input capacitance C_{in} can be significantly reduced from 20pF [5] to 2pF in our work. Moreover, reducing input capacitance, C_{in} also helps improving input impedance Z_{in}.

Due to chopping V_{in}, the input impedance Z_{in} is reduced, leading to electrode-tissue damaged [10]. A positive feedback loop (PFL) [6] is used to improve the input impedance. The PFL includes a chopper CH_{pf} and capacitors $C_{pf1,2}$. In our work, $C_{pf1,2}$ of 100fF is realized with a chopping frequency of 10kHz. Owing to the mismatch process during chip implementation, the G_{m1} is associated with an intrinsic offset V_{OS1}, as shown in Fig. 1. V_{OS1} is chopped to chopping frequency by CH_{out} then created the output ripple, which is filtered out by the off-chip post low pass filter.

The proposed CCIA is realized using a 180nm CMOS process. The layout of the proposed CCIA is shown in Fig. 2. It occupies the active silicon area of 0.22 × 0.38mm^2. Therefore, this design can be used for the implantable applications to record neural signal. According to the post-layout simulation, the closed-loop gain shown in Fig. 3 (a) achieves 40 dB with its bandwidth up to 2.5kHz. When DSL-BC is enabled, the high pass corner is successfully created at low frequency. As shown in Fig. 3 (b), the integrated input-referred noise (IRN) over a bandwidth of BW = 1 - 200Hz is 2.4μV_{rms} with a noise density of 172nV/√Hz and a 1/f corner of 2Hz. The power consumption of this work is only 1μW. Therefore, the noise efficiency factor NEF, introduced in [12], is calculated as:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{DC}}{\pi V_{th} 4kT \times BW}} \approx 6.6 \quad (3)$$

where $V_{ni,rms}$ is input-referred noise, I_{DC} is the amplifier's total current consumption, V_{th} is the thermal voltage, and BW is the amplifier's bandwidth.

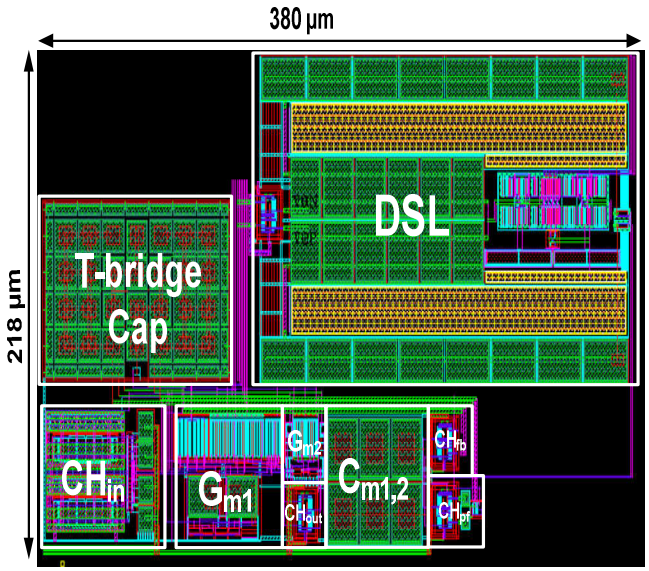
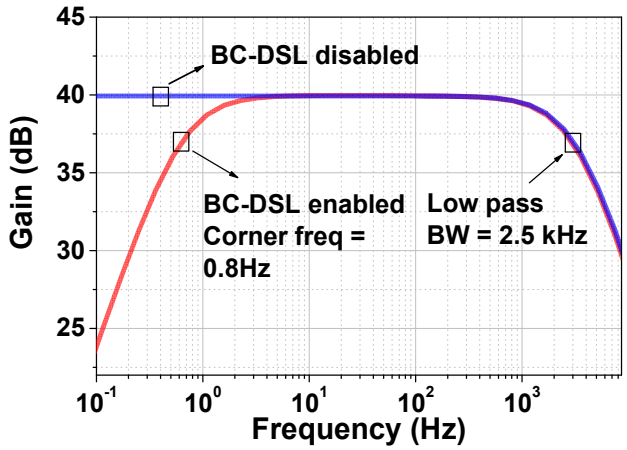
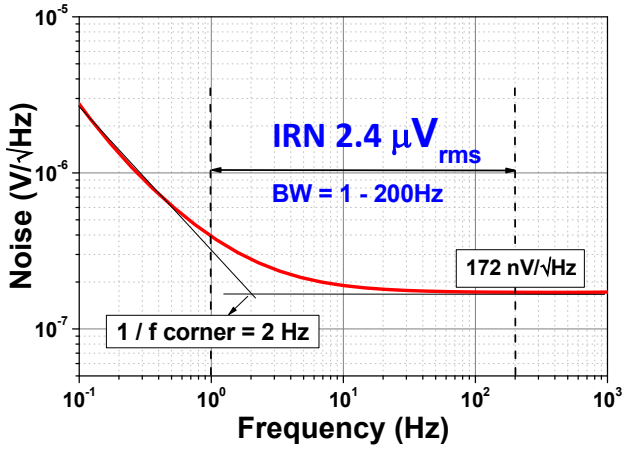


Figure 2. The layout of the proposed CCIA



(a)



(b)

Figure 3. Post layout simulated results of the proposed CCIA:

(a) The closed-loop gain; (b) The input-referred noise

3. CONCLUSION

The paper presents the proposed CCIA using DSL-BC and low input capacitance for the bio-medical application. The CCIA is implemented by 180nm CMOS technology. This chip consumes only 1μA from 1V supply to achieve an IRN of 2.4μV_{rms} over the bandwidth of 200Hz. Therefore, the NEF of 6.6 of the proposed CCIA is achieved. The V_{EOS} is successfully addressed by DSL-BC. Moreover, the T-bridge network capacitance is utilized in the negative feedback loop; hence, using the low input capacitance can significantly save the silicon area.

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THÔNG TIN TÁC GIẢ

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