A NEW BUCK-BOOST CONVERTER WITH HIGH VOLTAGE CONVERSION RATIO AND REDUCED VOLTAGE AND CURRENT STRESS ON SWITCHES AND DIODES

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Abstract

This article presents an improved buck-boost converter configuration capable of achieving a high voltage conversion ratio while significantly reducing voltage and current stresses on key components such as MOSFETs and diodes. The proposed design not only enhances operational efficiency but also optimizes system reliability. To provide an objective evaluation, experimental tests were conducted to compare voltage overshoot across switching components, including switches and diodes, relative to the output voltage and to analyze the current overshoot ratio of switches and diodes concerning the input current. Additionally, the overall efficiency of the proposed converter was assessed against existing designs, considering the impact of parasitic resistances in the components. Simulation and experimental results validate the theoretical analysis and demonstrate that the proposed topology outperforms conventional two-switch buck-boost converters in mitigating voltage and current stresses on critical elements. With these advantages, the proposed design holds strong potential for applications demanding high efficiency and long-term stability.

Keywords: *Buck-boost; non-isolated; voltage gain; negative output; current stress.*

1. Introduction

DC-DC voltage converters are crucial in various applications, particularly renewable energy systems. Standard DC-DC converters, such as boost, buck, and buck-boost, are widely utilized in photovoltaic (PV) systems because they regulate the output voltage according to fluctuating input conditions. Among them, the buck-boost converter offers flexibility but is limited by parasitic resistance when high voltage gain is required. Alternative topologies like the Cuk converter have been developed to address this limitation, offering flexible operation in step-up and step-down modes depending on the switching duty cycle [1], [2]. The Cuk converter is notable for its continuous output current and high efficiency, though its voltage gain remains constrained.

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Second-order DC-DC converter topologies have been introduced to overcome this issue, providing higher voltage gain. Studies [3]-[8] have proposed various second-order converter structures, including enhanced versions of the Cuk converter. The improved topology in [5] ensures continuous input current, albeit with significant current ripple. The topology in [4] suffers from high voltage stress on switching devices. At the same time, the one in [7] achieves continuous input and output currents but requires different types of switches (NMOS and PMOS), complicating gate drive circuitry. In [8], another second-order converter was introduced with superior voltage gain compared to previous designs; however, it maintains a continuous input current while the output current remains discontinuous. However, these topologies share a common drawback: the voltage and current across key components, including power switches and diodes, often exceed input and output levels. This excessive electrical stress can degrade or damage sensitive components such as switches, diodes, and capacitors [9], [10]. High voltage and current levels also contribute to energy losses due to heat dissipation, ultimately reducing conversion efficiency [11]. Moreover, mitigating voltage and current stresses enables the use of more compact components, leading to space savings, reduced design weight, and cost optimization in DC-DC converter development [12], [13].

In summary, researching and developing new circuit topologies for non-isolated buck-boost DC-DC converters to reduce voltage and current stresses is essential for ensuring high efficiency, durability, and applicability in modern energy systems. Therefore, this study proposes a converter that achieves high voltage gain while reducing voltage and current stresses on the switches and diodes, ensuring operational safety and prolonging the power components' lifespan.

2. Proposed topology

2.1. Proposed converter topology

The proposed converter topology, as shown in Fig. 1, consists of two inductors (L1 and L2), three capacitors (C1, C2, and Co), two switches (S1 and S2), and three diodes (D1, D2, and D3). The power switches operate synchronously, resulting in two operating modes: the first mode, when the switches are turned on, is illustrated in Fig. 2, while the second mode, when the switches are turned off, is depicted in Fig. 3.

2.2. Operating mode

The first operating mode occurs when both switches are turned on, as illustrated in Fig. 2. In this mode, the current of inductor L1 flows through switch S1, while the current of inductor L2 flows through switch S2. The electric fields of capacitors C1, C2, and Co release energy. The voltage across all inductors is positive, allowing their magnetic fields to store energy.

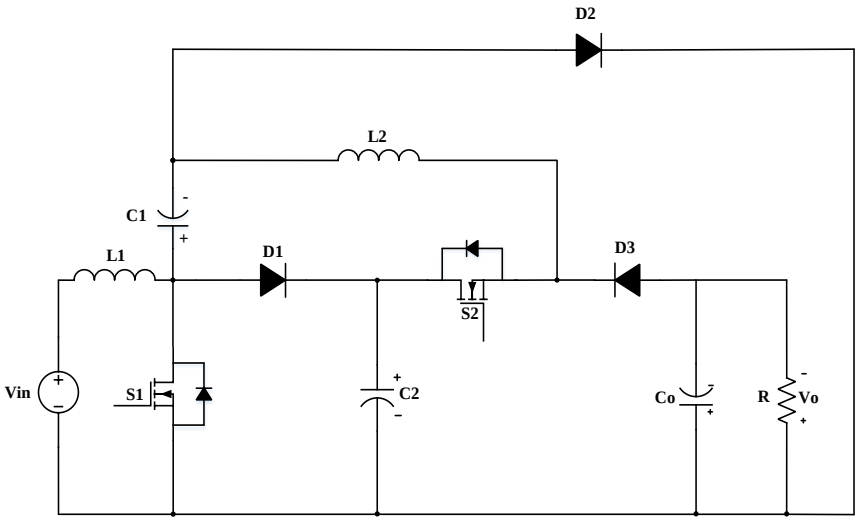

Fig. 1. Proposed converter.

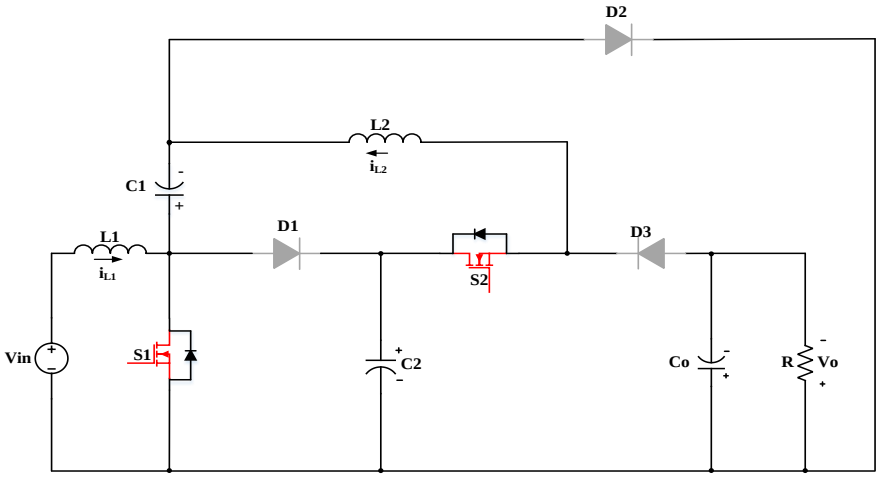

Fig. 2. Operating stage 1.

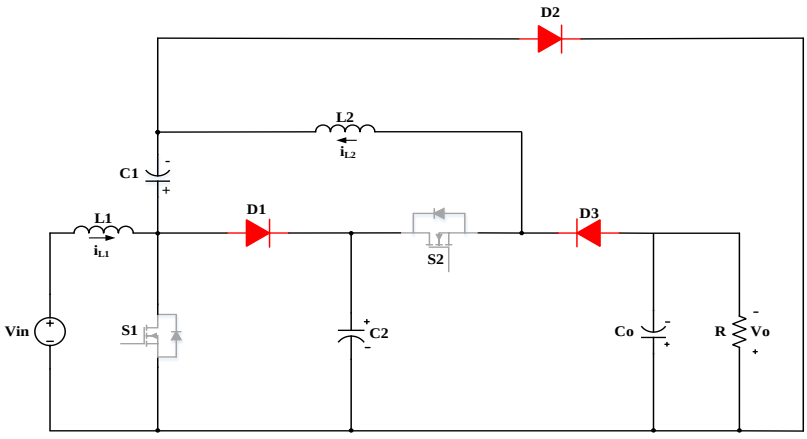

Fig. 3. Operating stage 2.

The second operating mode occurs when both switches are turned off, as illustrated in Fig. 3. In this mode, the current flowing through the inductors forward-biases the diodes, causing the voltage across the inductors to become negative, leading to demagnetization and the release of stored energy. The capacitors are charged during this mode, storing energy in their electric fields.

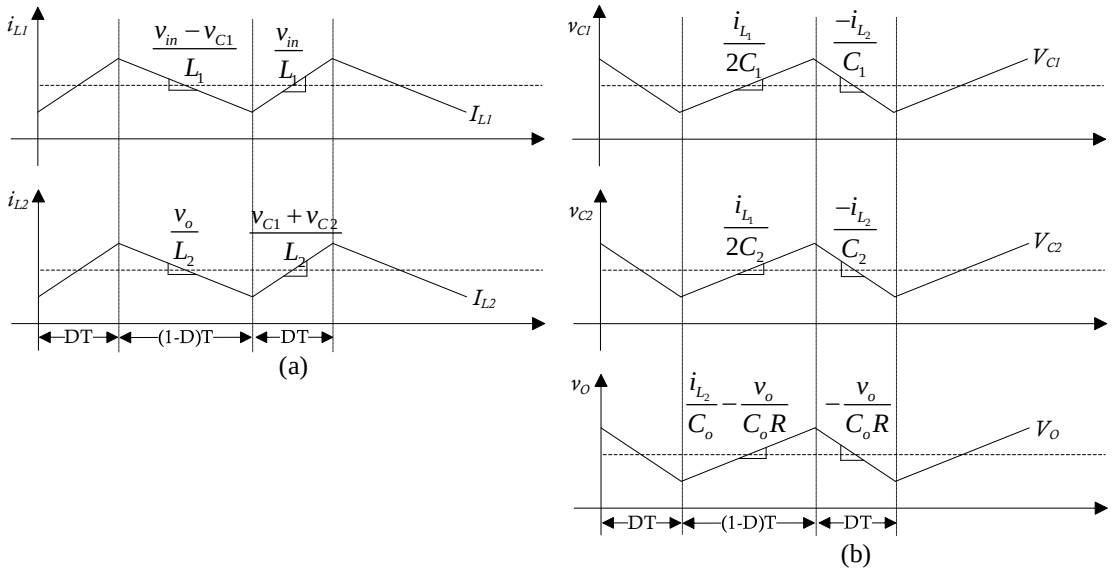

Fig. 4. Time-domain waveforms of the proposed converter: (a) Inductor voltage, (b) Capacitor current.

Figure 4 presents the voltage and current waveforms of the inductors and currents through the semiconductor components based on the proposed concepts. The expressions for the voltage across the inductors and the currents through the capacitors are given in (1)

$$\begin{cases} L1\dfrac{d_{i_{L1}}}{dt} = D\left(V_{in}\right)+\left(1-D\right)\left(V_{in}-V_{C1}\right) \\ L2\dfrac{d_{i_{L2}}}{dt} = D\left(V_{C1}+V_{C2}\right)+\left(1-D\right)\left(V_o\right) \\ C1\dfrac{d_{V_{C1}}}{dt} = D\left(-i_{L2}\right)+\left(1-D\right)\left(\dfrac{i_{L1}}{2}\right) \\ C2\dfrac{d_{V_{C2}}}{dt} = D\left(-i_{L2}\right)+\left(1-D\right)\left(\dfrac{i_{L1}}{2}\right) \\ C_o\dfrac{d_{V_{Co}}}{dt} = D\left(-\dfrac{V_o}{R}\right)+\left(1-D\right)\left(i_{L2}-\dfrac{V_o}{R}\right) \end{cases} \quad (1)$$

2.3. Voltage conversion ratio

In steady-state operation, the average voltage across the inductors over one switching cycle is zero. This results in the inductor voltage Eq. (1) equating to zero. Consequently, the average voltage across the capacitors can be expressed as shown:

$$V_{C1} = V_{C2} = \frac{(D-1)V_o}{2D} = \frac{V_{in}}{1-D}, V_o = -\frac{2D}{(1-D)^2}V_{in}. \quad (2)$$

Thus, the voltage conversion ratio of the proposed converter can be derived from (2), and its expression is given (3)

$$M = \frac{V_o}{V_{in}} = -\frac{2D}{(1-D)^2}. \quad (3)$$

2.4. Average current through the inductors

The symmetry of the final expression implies a balance between charge and time, meaning the capacitors operate as open circuits. This concept refers to the average current of the capacitors being zero over a switching cycle. Therefore, the current relationship of the capacitors in (1) becomes zero, and as a result, the average current of the inductors can be represented by (4)

$$I_{L1} = \frac{2D}{(1-D)^2} I_o,\ I_{L2} = \frac{I_o}{1-D},\ I_o = \frac{V_o}{R}. \quad (4)$$

2.5. Voltage stress on the switch and diode

The average current through the semiconductor components and the voltage applied to the semiconductor components during the off-state or non-operating period are determined. Therefore, the voltage stress values of the semiconductor components can be expressed by (5)

$$\begin{cases} V_{S1} = V_{D1} = V_{D2} = \dfrac{V_{in}}{1-D} = -\dfrac{(1-D)V_o}{2D} \\ V_{S2} = V_{D3} = \dfrac{(1+D)V_{in}}{(1-D)^2} = -\dfrac{(1+D)V_o}{2D} \end{cases}. \quad (5)$$

According to the operating principle, the current through the power switch S1 can be expressed by (6)

$$I_{S1} = \frac{DI_o(1+D)}{(1-D)^2} \quad (6)$$

Therefore, the average value of I_{S1} can be calculated as (7)

$$I_{S1} = \frac{DI_o\left(1+D\right)}{\left(1-D\right)^2} \tag{7}$$

Similarly, the average value of the current through the switch *S*2 is determined by (8)

$$I_{S2} = \frac{DI_o}{1-D} \tag{8}$$

From the operating stages, the current through the diode *D*1 can be expressed by (9)

$$i_{D1} = \begin{cases} 0 & \left(NT, NT+DT\right) \\ \frac{i_{L1}}{2} & \left(NT+DT, NT+T\right) \end{cases} \tag{9}$$

Therefore, the average value of I_{D1} can be given by (10)

$$I_{D1} = \frac{DI_o}{1-D}. \tag{10}$$

Similarly, the average value of the current through diodes *D*2 and *D*3 is inferred as follows (11)

$$I_{D2} = \frac{I_o}{1-D};\ I_{D3} = I_o. \tag{11}$$

2.6. Ripple of current and voltage

From the waveforms in Fig. 2, we can observe that the current through the inductor i_{L1} increases during the first time interval (*DT*) and then decreases during the second time interval (1-*D*)*T*. Therefore, the peak-to-peak current ripple and the variation of the current Δi_{L1} can be calculated as (12)

$$\Delta i_{L1} = \frac{V_{in}DT}{L_1};\ \zeta_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{\left(1-D\right)^2 TR}{4\left|M\right|L1}. \tag{12}$$

Furthermore, the peak-to-peak current ripple and the variation of the current Δi_{L2} are calculated as follows (13)

$$\Delta i_{L2} = \frac{\left(V_{C_1}+V_{C_2}\right)DT}{L2} = \frac{2DV_{in}T}{\left(1-D\right)L2};\ \zeta_2 = \frac{\Delta i_{L2}/2}{I_{L2}} = \frac{DTR}{\left|M\right|L2} \tag{13}$$

The peak-to-peak voltage ripple and the variation of the voltages ΔV_{C1}, ΔV_{C2}, and

ΔV_{Co} can be inferred, and their related expressions are presented in (14) and (15)

$$\Delta V_{C1} = \Delta V_{C2} = \frac{\Delta Q}{C} = \frac{I_{L2} DT}{C} = \frac{2D^2 T V_{in}}{(1-D)^3 RC}; \zeta_C = \frac{\Delta V_C / 2}{V_C} = \frac{2D^3 T}{(1-D)^4 |M| RC} \quad (14)$$

$$\Delta V_{Co} = \frac{\Delta Q}{C} = \frac{IoDT}{C_o} = \frac{2D^2 T V_{in}}{(1-D)^2 RC_o}; \zeta_{Co} = \frac{\Delta V_{Co} / 2}{V_{Co}} = \frac{D^2 T}{(1-D)^2 |M| RC_o} \quad (15)$$

where $C1 = C2 = C.$

2.7. Boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM)

The boundary between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is defined when the minimum value of the inductor current reaches zero, corresponding to $IL_1 = \frac{\Delta iL_1}{2}$ and $IL_2 = \frac{\Delta iL_2}{2}$. By substituting Eqs. (4), (12), and (13) into these two expressions, the condition for the proposed converter to operate in continuous conduction mode can be derived as Eq. (16)

$$L_1 > \frac{(1-D)^4 TR}{8D}; L_2 > \frac{(1-D)^2 TR}{2} \quad (16)$$

3. Power loss analysis

3.1. Inductor losses

The power loss of the inductor includes copper loss due to the winding resistance r_L and core losses caused by hysteresis and eddy currents. Copper loss plays a significant role in the total power dissipation of the inductor.

The approximate *RMS* values of the inductor currents are determined as given in (17)

$$I_{L1(rms)} = \sqrt{\frac{\int_0^T i_{L1}^2(t)\,dt}{T}} \approx \frac{2D}{(1-D)^2} I_o; I_{L2(rms)} = \sqrt{\frac{\int_0^T i_{L2}^2(t)\,dt}{T}} \approx \frac{I_o}{1-D}. \quad (17)$$

The copper loss of the inductors can be calculated as follows (18)

$$P_{L\_Cu} = I_{L1(rms)}^2 r_{L1} + I_{L2(rms)}^2 r_{L2} = \left(\frac{4D^2}{(1-D)^4} \frac{r_{L1}}{R} + \frac{1}{(1-D)^2} \frac{r_{L2}}{R} \right) P_o. \quad (18)$$

The core loss density of the inductor can be estimated from the magnetization

curve, following the loss expression (19)

$$\Delta P_{L\_Co} = aB^b f^c. \tag{19}$$

where *a*, *b*, and *c* are determined from the magnetization curve data based on specifications, and *B* is defined as half the amplitude of the *AC* magnetic flux variation. Therefore, the core loss of the inductors is calculated as given in (20)

$$P_{L\_Co} = l_{e1}A_{e1}\Delta P_{L1\_Co} + l_{e2}A_{e2}\Delta P_{L2\_Co}. \tag{20}$$

where l_e is the path length and A_e is the cross-sectional area of the magnetic core.

Therefore, the total power loss of the inductor is the sum of core loss and copper loss, expressed as (21)

$$P_L = P_{L\_Cu} + P_{L\_Co}. \tag{21}$$

3.2. Capacitor losses

The power loss of the capacitor is caused by the parasitic resistance r_C. Based on the instantaneous current in different operating stages, the approximate *RMS* value of the capacitor current can be given by (22) and (23)

$$I_{C1(rms)} = I_{C2(rms)} = \sqrt{\frac{\int_0^{DT} i_{L2}^2(t)\,dt + \int_{DT}^{T} \frac{i_{L1}^2}{4}(t)\,dt}{T}} = \frac{I_o\sqrt{D}}{(1-D)\sqrt{1-D}} \tag{22}$$

$$I_{Co(rms)} = \sqrt{\frac{\int_0^{DT} i_o^2(t)\,dt + \int_{DT}^{T} (i_{L2}-i_o)^2(t)\,dt}{T}} = \sqrt{DIo + \frac{(DI_o)^2}{1-D}}. \tag{23}$$

The power loss of the capacitors can be calculated using the following expression (24)

$$P_C = I_{C1(rms)}^2 r_{C1} + I_{C2(rms)}^2 r_{C2} + I_{Co(rms)}^2 r_{Co} = \left(\frac{D}{(1-D)^3}\frac{2r_C}{R} + \left(\frac{D}{I_o} + \frac{D^2}{1-D}\right)\frac{r_{Co}}{R}\right)P_o \tag{24}$$

where $r_{C1} = r_{C1} = r_C$.

3.3. Switching loss

Power loss includes conduction loss due to the on-state resistance r_{DS} when the switch is turned on and switching loss occurring during the rise time t_r and fall time t_f.

The conduction loss of switches S1 and S2 depends on r_{DS} and the *RMS* value of the switch currents. Based on the instantaneous currents in different operating stages, the approximate *RMS* values of the switch currents are determined as given in (25)

$$I_{S1(rms)} = \sqrt{\frac{\int_0^{DT} \left(i_{L1} + i_{L2}\right)^2 dt}{T}} \approx \frac{\sqrt{D}\left(1+D\right) I_o}{\left(1-D\right)^2};\ I_{S2(rms)} = \sqrt{\frac{\int_0^{DT} \left(i_{L2}\right)^2 dt}{T}} \approx \frac{\sqrt{D} I_o}{1-D}. \quad (25)$$

The conduction loss of the power switches is calculated as given by (26)

$$P_{S\_C} = I_{S1(rms)}^2 r_{DS1} + I_{S2(rms)}^2 r_{DS2} = \left(\frac{\left(1+D\right)^2 D}{\left(1-D\right)^4} \frac{r_{DS1}}{R} + \frac{D}{\left(1-D\right)^2} \frac{r_{DS1}}{R} \right) P_o. \quad (26)$$

The switching loss of a power switch is related to the rise time, fall time, voltage stress, and the average current through the switch. Therefore, the switching loss of power switches can be expressed as follows (27):

$$P_{S\_S} = \frac{1}{2} V_{S1} I_{S1} \left(t_{r1} + t_{f1}\right) f_{S1} + \frac{1}{2} V_{S2} I_{S2} \left(t_{r2} + t_{f2}\right) f_{S2} = \left(\frac{\left(1-D^2\right)\left(t_{r1} + t_{f1}\right) f_{S1} + \left(1+D\right)\left(t_{r2} + t_{f2}\right) f_{S2}}{4\left(1-D\right)} \right) P_o \quad (27)$$

Therefore, the total power loss of the power switches is the sum of the losses during conduction and switching, as shown in the expression (28)

$$P_S = P_{S\_C} + P_{S\_S}. \quad (28)$$

3.4. Power losses of diodes

The loss of the diode is primarily due to the forward voltage V_F and the series resistance r_D. Based on the instantaneous currents in the different operating stages, the approximate *RMS* values of the current through the diodes can be calculated as follows (29)

$$I_{D1(rms)} = \sqrt{\frac{\int_{DT}^{T} \left(\frac{i_{L1}}{2}\right)^2 dt}{T}} \approx \frac{D I_o}{\left(1-D\right)^{3/2}};\ I_{D2(rms)} = \sqrt{\frac{\int_{DT}^{T} \left(\frac{i_{L1}}{2} + i_{L2}\right)^2 dt}{T}} \approx \frac{I_o}{\left(1-D\right)^{3/2}};\ I_{D3(rms)} = \sqrt{\frac{\int_{DT}^{T} \left(i_{L2}\right)^2 dt}{T}} \approx \frac{I_o}{\sqrt{1-D}}. \quad (29)$$

Therefore, the expression for the power loss of the diodes is given by (30):

$$\begin{aligned} P_D &= I_{D1} V_{F1} + I_{D2} V_{F2} + I_{D3} V_{F3} + I_{D1(rms)}^2 r_{D1} + I_{D2(rms)}^2 r_{D2} + I_{D2(rms)}^2 r_{D2} \\ &= \left(\frac{D V_{F1}}{\left(1-D\right)\left|V_o\right|} + \frac{V_{F2}}{\left(1-D\right)\left|V_o\right|} + \frac{V_{F3}}{\left|V_o\right|} + \frac{D^2}{\left(1-D\right)^3} \frac{r_{D1}}{R} + \frac{1}{\left(1-D\right)^3} \frac{r_{D2}}{R} + \frac{1}{1-D} \frac{r_{D3}}{R} \right) P_o. \end{aligned} \quad (30)$$

4. Calculated efficiency

The total power loss of the proposed converter is the sum of the power losses of the inductors, capacitors, power switches, and diodes. It can be calculated as follows (31)

$$P_{Loss} = P_L + P_C + P_S + P_D. \quad (31)$$

Therefore, the calculated efficiency of the proposed converter is given by the following (32)

$$\eta = \frac{P_o}{P_o + P_L + P_C + P_S + P_D}. \quad (32)$$

5. Comparison with other buck-boost converters

In Tab. 1, the proposed converter demonstrates superiority over the converters studied in the references. The voltage stress factor of switch S1, diodes D1, and D2 is the lowest among the converters in [3]-[8], at only 61% of the output voltage, while for switch S2, this factor is 2% higher compared to [3], [4] and [6], [7]. For diode D3, since the converters in [3]-[8] do not use this diode, there is no direct comparison, but this study also shows that the voltage across diode D3 exceeds the output voltage by 61%.

Tab. 1. Comparison of the normalized voltage stress across semiconductor components with a voltage step-up ratio is 3

Converters	$\frac{V_{S1}}{V_o}$	$\frac{V_{S2}}{V_o}$	$\frac{V_{D1}}{V_o}$	$\frac{V_{D2}}{V_o}$	$\frac{V_{D3}}{V_o}$	D
[3]	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	-	0.63
[4]	$\frac{1}{D^2}=2.51$	$\frac{1}{D}=1.59$	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	-	0.63
[5]	$\frac{1-D}{D^2}=0.93$	1	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	-	0.63
[6]	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	$\frac{1}{D}=1.59$	$-\frac{1}{D^2}=2.51$	-	0.63
[7]	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	$\frac{1-D}{D^2}=0.93$	$\frac{1}{D}=1.59$	-	0.63
[8]	1	1	1	1	-	0.56
Proposed	$\frac{1-D}{2D}=0.61$	$\frac{1+D}{2D}=1.61$	$\frac{1-D}{2D}=0.61$	$\frac{1-D}{2D}=0.61$	$\frac{1+D}{2D}=1.61$	0.45

In DC-DC converters, the normalized voltage stress factor is the voltage ratio across the power switch to the output voltage, reflecting how much the voltage on the power switch exceeds the output voltage. This is an important indicator for evaluating the efficiency and durability of the converter. A low voltage stress factor typically indicates that the power switch operates more efficiently, thereby improving

performance and extending the lifespan of the components.

Similarly, Tab. 2 highlights the advantages of the proposed converter configuration by analyzing the current stress index of semiconductor components relative to the input current. Notably, for switch S1, this index is 27% lower than in [3]-[8], indicating reduced electrical stress and improved longevity.

Tab. 2. Comparison of the normalized current stress across semiconductor components with a voltage step-up ratio of 3

Converters	$\left\|\frac{I_{S1}}{I_{in}}\right\|$	$\left\|\frac{I_{S2}}{I_{in}}\right\|$	$\left\|\frac{I_{D1}}{I_{in}}\right\|$	$\left\|\frac{I_{D2}}{I_{in}}\right\|$	$\left\|\frac{I_{D3}}{I_{in}}\right\|$	D
[3]	1	$\frac{1-D}{D}=0.59$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.34$	-	0.63
[4]	1	$\frac{1-2D}{D}=0.41$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.34$	-	0.63
[5]	1	$\frac{1-D}{D}=0.59$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.34$	-	0.63
[6]	1	$\frac{1-D}{D}=0.59$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.34$	-	0.63
[7]	1	$\frac{1-D}{D}=0.59$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.34$	-	0.63
[8]	1	$1-D=0.44$	$\frac{1-D}{D}=0.59$	$\left(\frac{1-D}{D}\right)^2=0.35$	-	0.56
Proposed	$\frac{1+D}{2}=0.73$	$\frac{1-D}{2}=0.28$	$\frac{1-D}{2}=0.28$	$\frac{1-D}{2D}=0.61$	$\left(\frac{1-D}{D}\right)^2=0.34$	0.45

Moreover, the superiority of the proposed design is further emphasized by the lowest current stress index observed for diode D1 compared to other converters. In contrast, the current stress index for S2 exceeds the input current is 31% lower than the configurations in [3] and [5]-[7], 16% compared to [8], and 13% compared to [4]. Additionally, the overcurrent ratio for diode D3 relative to the input current remains low at only 34%.

Due to the combined influence of currents L1 and L2 in stage 2, the overshoot in diode D2 is the highest among the studied converters but remains at a manageable 61%. These characteristics collectively contribute to the proposed converter's enhanced efficiency, extended component lifespan, and improved heat dissipation, leading to excellent system reliability and stability.

Table 3 provides a detailed comparison of the number of components used in different converter topologies and their corresponding voltage gain. The proposed

converter incorporates one diode compared to the other designs, contributing to its enhanced performance characteristics.

Despite this slight increase in component count, the proposed converter achieves the highest voltage transformation ratio among the compared configurations. This indicates its superior capability to boost voltage levels efficiently while maintaining operational stability. The optimized design ensures that the additional component does not introduce significant complexity but enhances overall performance, making it a favorable choice for high-voltage applications.

Tab. 3. Compare elements in configurations and voltage gain

Converters	**L**	**C**	**S**	**D**	**Total**	**Voltage gain**
Proposed	2	3	2	3	10	$\frac{2D}{(1-D)^2}$
[3]	2	2	2	2	8	$\left(\frac{D}{1-D}\right)^2$
[4]	3	3	2	2	10	$\left(\frac{D}{1-D}\right)^2$
[5]	3	3	2	2	10	$\left(\frac{D}{1-D}\right)^2$
[6]	2	2	2	2	8	$\left(\frac{D}{1-D}\right)^2$
[7]	3	3	2	2	10	$\left(\frac{D}{1-D}\right)^2$
[8]	2	2	2	2	8	$\frac{D}{(1-D)^2}$

To objectively assess the efficiency of the proposed converter, a comprehensive evaluation was conducted, comparing its performance with other buck-boost converters referenced in [3]-[8]. The experiments were designed to simulate real-world operating conditions where the converters were significantly affected by the parasitic resistances of inductors, diodes, and power switches. The parasitic resistance was set at 0.003 times the load resistance to account for practical losses.

For a fair and precise comparison, all converters were configured with identical component specifications in Tab. 4: 47 µF capacitors, 0.4 mH inductors, DC input voltage of 24 V, a load resistance 80 Ω. Additionally, the switching devices' on-state resistance (R_{DS}) was standardized at 4.8 mΩ. By maintaining consistent test

conditions, the evaluation ensured a reliable assessment of efficiency, highlighting the proposed converter's superior performance and operational benefits.

The results presented in Fig. 5 highlight the superior performance of the proposed converter in terms of efficiency. It achieves maximum efficiency of 99.09% and maintains a minimum of 93.68% while operating stably across a broad power range from 6 W to 806 W. This demonstrates its ability to sustain high efficiency over varying load conditions.

Tab. 4. Element parameters

Elements	Value	Unit
Capacitors	47	uF
Inductors	0.4	mH
Load	80	Ω
DC Source	24	V
Switching frequency	25	kHz

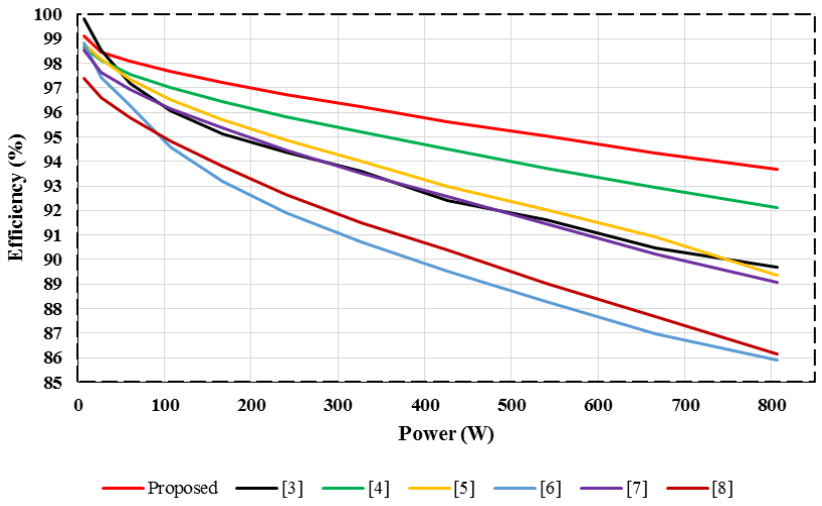

Fig. 5. Compare the performance of the proposed converter with other buck-boost converters.

In comparison, the converters discussed in [3]-[8] exhibit lower overall efficiency. While the converter in [3] shows an advantage in low-power applications, specifically in the range of 6 W to 26 W, where it reaches a peak efficiency of 99.79%, its performance declines significantly as power increases, ultimately falling below that of the proposed

converter. This efficiency drop limits its effectiveness in high-power applications.

Notably, at a power level of 540 W, the proposed converter maintains a high efficiency of 95.04%. This represents a significant improvement over other designs, with an efficiency increase of 3.59% compared to [3] and [7], 1.33% higher than [4], 2.99% greater than [5], and an impressive 6.73% improvement over [6]. These comparisons emphasize the effectiveness of the proposed converter in delivering consistently high efficiency across a wide operating range, making it a strong candidate for applications requiring high power and energy efficiency.

The efficiency analysis indicates that reducing voltage and current stresses on the power switch and diode in the proposed converter significantly enhances overall efficiency despite switching and conduction losses. Specifically, lowering the voltage stress on the power switch and diode reduces switching and diode losses, as described in Eqs. (27) and (30) analyzed in Section 3. Since the voltage across the switch and diode is directly proportional to power losses in these components, minimizing voltage stress is crucial in improving the converter's efficiency. Additionally, conduction losses in the power switch are proportional to the square of its RMS current, as expressed in Eq. (26). Therefore, reducing current stress also contributes significantly to optimizing the overall efficiency of the converter.

6. Simulation and experimental results

Simulation experiments were conducted using the PSIM environment to verify the accuracy of the theoretical analyses presented in Section 2, 3, 4, and 5. Additionally, to validate the proposed topology, experimental tests were performed on a hardware prototype to analyze voltage and current stresses on the switches and diodes. The setup parameters for both simulations and experiments are provided in Tab. 4.

Figure 6 presents the simulation results at a duty cycle of D = 0.5, demonstrating strong agreement with Eqs. (7), (8), (10), and (11), as well as the input current overshoot expressions listed in Tab. 2. Specifically, the average current through switch S1 is 3.6A, while switch S2 maintains 1.19 A. The current through diodes D1, D2, and D3 measures 1.22 A, 2.44 A, and 1.22 A, respectively.

Likewise, Fig. 7 confirms that the theoretical expressions derived in Section 2 to 5, along with the voltage stress values on diodes and capacitors detailed in Tab. 1,

closely match the simulation results. Specifically, the voltage across switches S1 and S2 is 48.39 V and 144.96 V, respectively. The reverse voltage across diodes D1 and D2 is 48.49 V, while diode D3 experiences a reverse voltage of 144.96 V.

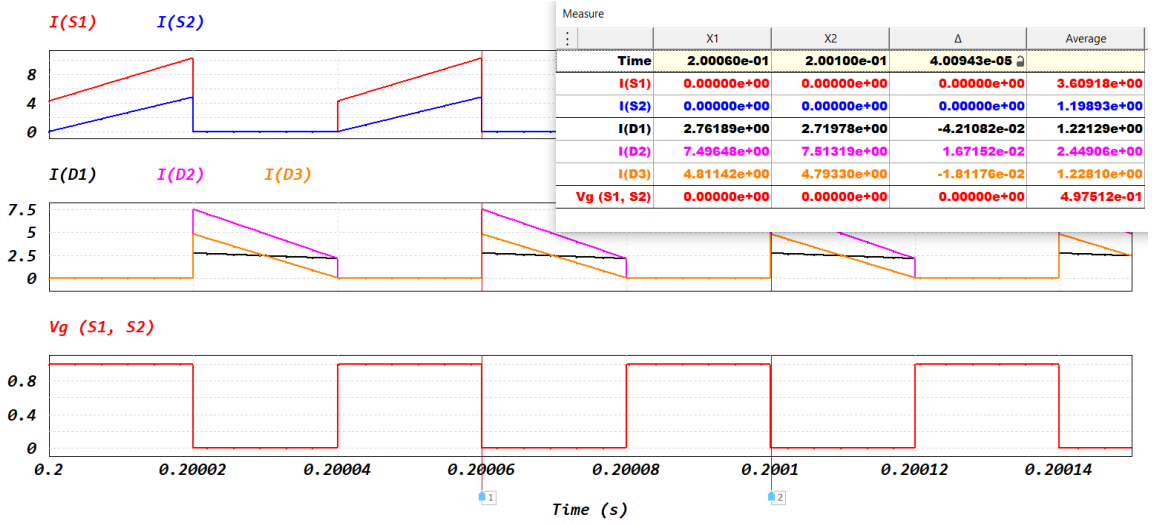

Fig. 6. Current stress on switches and diodes.

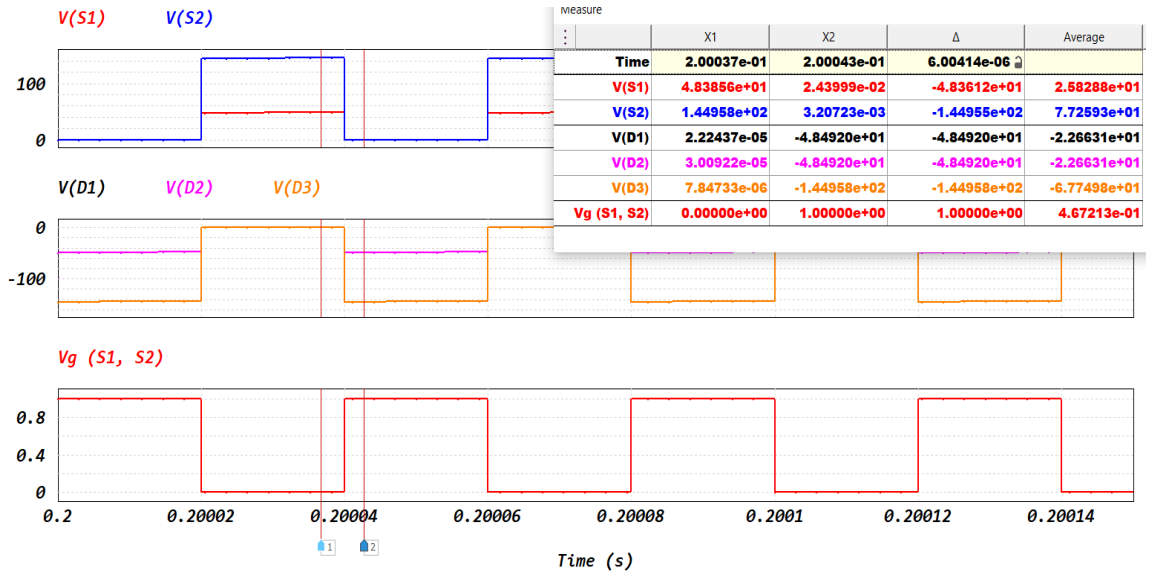

Fig. 7. Voltage stress on switches and diodes.

As shown in Fig. 8, an experimental prototype was implemented to further clarify the theoretical analyses, with setup parameters in Tab. 4.

The measured voltage waveforms across the switches and diodes, illustrated in

Fig. 9, indicate that the peak voltage on S1 is approximately 50 V, while S2 reaches around 150 V. The reverse voltage across D1 and D2 is nearly identical, fluctuating around 50 V, whereas D3 experiences a reverse voltage of approximately 150 V.

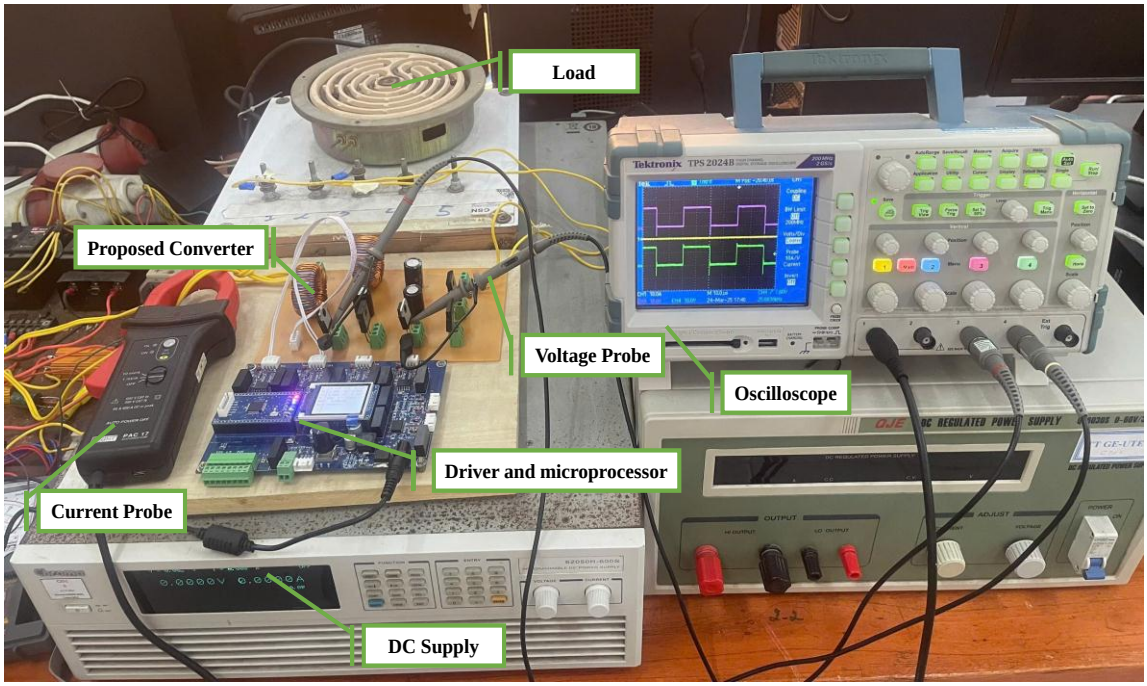

Fig. 8. Experimental model.

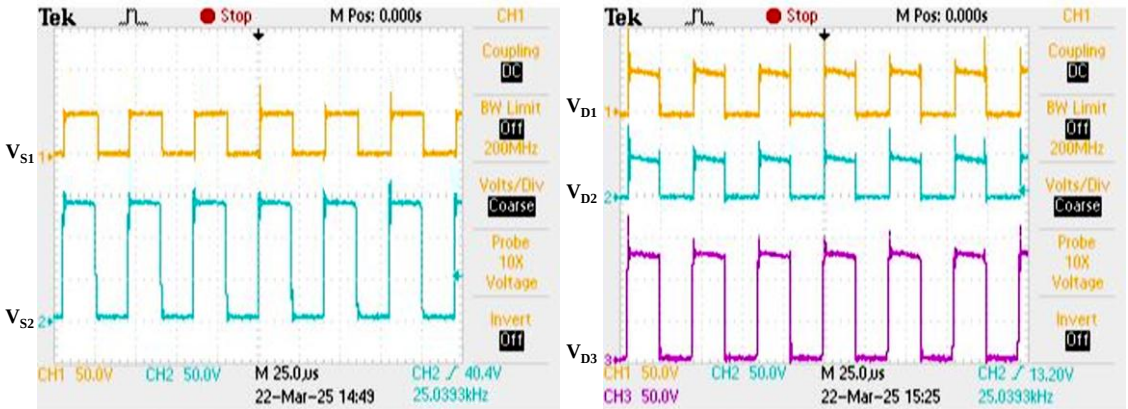

Fig. 9. Voltage stress on switches and diodes.

Figure 10 reveals minor discrepancies between the experimental and simulated current results, primarily due to the influence of parasitic resistance and capacitance in the switching devices. However, the overall agreement remains strong. Specifically, the average current through S1 is 3.8 A, while S2 carries 2 A. The diodes' measured currents through D1, D2, and D3 are 1.42 A, 3.1 A, and 1.45 A, respectively.

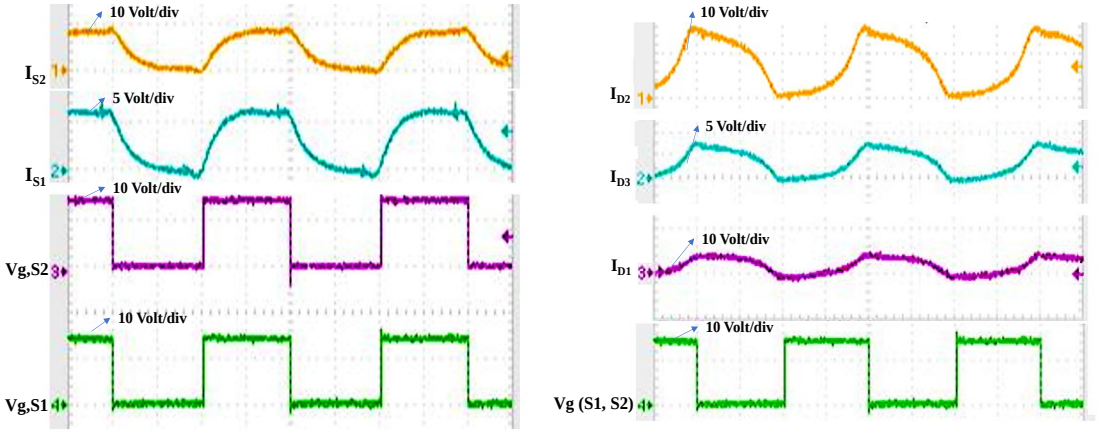

Fig. 10. Current stress on switches and diodes.

7. Conclusion

This study proposes an improved buck-boost converter configuration capable of achieving a high voltage conversion ratio, outperforming existing designs referenced in [3]-[8]. The proposed converter exhibits the lowest voltage stress on the main switch S1 and diodes D1 and D2. Furthermore, the current overshoot ratio relative to the input current is optimized, with the lowest values observed for switch S1 and diode D1, while S2 and D2 exhibit variations depending on specific operating conditions. This demonstrates the converter’s ability to significantly reduce voltage and current stresses, enhancing efficiency, extending component lifespan, and improving system reliability. Simulation evaluations validate the superiority of the proposed configuration, achieving a peak efficiency of 99.09% at a voltage gain of 3 while maintaining stable operation over a wide power range from 6 W to 806 W. Notably, its efficiency surpasses that of other converters, particularly in the 60W to 806W range. Simulation and experimental results closely align with theoretical analysis, further confirming the feasibility of the design. With these advantages, the proposed converter holds strong potential for practical applications in power systems requiring high voltage conversion ratios and superior efficiency.

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BỘ CHUYỂN ĐỔI BUCK-BOOST MỚI VỚI TỈ LỆ CHUYỂN ĐỔI ĐIỆN ÁP CAO VÀ GIẢM ỨNG SUẤT ĐIỆN ÁP VÀ DÒNG ĐIỆN TRÊN KHÓA ĐIỆN VÀ ĐI-ỐT

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Tóm tắt: Bài báo trình bày một cấu hình bộ chuyển đổi buck-boost cải tiến, có khả năng đạt tỉ lệ chuyển đổi điện áp cao trong khi giảm đáng kể điện áp stress và dòng điện stress trên các linh kiện quan trọng như MOSFET và đi-ốt. Thiết kế đề xuất không chỉ nâng cao hiệu suất hoạt động mà còn tối ưu hóa độ tin cậy của hệ thống. Để đánh giá khách quan, các thử nghiệm thực nghiệm đã được tiến hành nhằm so sánh mức độ vượt áp trên các linh kiện chuyển mạch, bao gồm các khóa điện và đi-ốt, so với điện áp đầu ra, đồng thời phân tích tỉ lệ vượt mức của dòng điện trên các linh kiện này so với dòng điện đầu vào. Ngoài ra, hiệu suất tổng thể của bộ chuyển đổi được đánh giá và đối chiếu với các thiết kế hiện có, có tính đến ảnh hưởng của điện trở ký sinh trong linh kiện. Kết quả mô phỏng và thực nghiệm xác nhận tính chính xác của phân tích lý thuyết, đồng thời chứng minh rằng cấu trúc đề xuất vượt trội hơn các bộ chuyển đổi buck-boost hai công tắc thông thường trong việc giảm điện áp stress và dòng điện stress trên các thành phần quan trọng. Với những ưu điểm này, thiết kế đề xuất hứa hẹn tiềm năng ứng dụng cao trong các hệ thống yêu cầu hiệu suất vượt trội và độ ổn định lâu dài.

Từ khóa: *Tăng-giảm áp; không cách ly; độ lợi cao; đầu ra đảo; ứng suất dòng điện.*

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