ENHANCED SEPIC CONVERTER REDUCES CURRENT STRESS ON SWITCHING DEVICES AND DIODES WHILE MAINTAINING HIGH EFFICIENCY

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Abstract

This article presents an innovative DC buck-boost converter design that mitigates the excessive switching current stress inherent in SEPIC converters. The study highlights a significant reduction in current strain on switching devices and diodes during transitions. A thorough steady-state analysis has been conducted, encompassing voltage conversion ratios, power dissipation, and voltage stress on key switching components. Simulation and theoretical evaluations in buck and boost modes demonstrate that the proposed converter achieves exceptionally low source current overshoot across switches S1, S2, D1, and D2, even when the conversion ratio varies from 0.2 to 2. Compared to SEPIC and other analyzed topologies, this converter delivers superior efficiency with substantially lower power losses. Furthermore, experimental validation, considering the impact of parasitic resistances, confirms that this design outperforms existing solutions by maximizing efficiency, enhancing reliability, minimizing energy dissipation, and extending operational lifespan, making it an optimal choice for power electronics applications. Moreover, experiments with nonlinear load currents were conducted further to validate the superior performance of the proposed converter.

Keywords: *Buck-boost converter; SEPIC converter; non-isolated; voltage gain; positive output.*

1. Introduction

Renewable energy sources have gained significant traction as fossil fuel reserves dwindle and environmental concerns escalate. These sustainable energy solutions offer a pathway to clean power generation without contributing to pollution. With numerous advantages, they are being rapidly adopted across various sectors. However, their output power remains highly dependent on weather and climatic conditions. Technologies like photovoltaic panels require DC-DC converters to regulate the output voltage, ensuring compatibility with loads or storage systems while meeting the voltage criteria for DC-AC conversion in grid-connected applications. DC-DC converters play a pivotal role in voltage adaptation for diverse electrical loads, which may require levels higher or lower

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DOI: 10.56651/lqdtu.jst.v21.n1.981

than the source voltage. To meet step-up and step-down demands efficiently, these converters must exhibit a streamlined architecture, high conversion efficiency, and precision control [1]. The advancement of semiconductor technology since the early 19th century has significantly propelled the widespread use of DC-DC converters in power electronics [1], [2].

DC-DC converters are indispensable in modern power conversion systems, facilitating seamless transitions between voltage levels. They find extensive applications in renewable energy systems, electric vehicles, uninterrupted power supplies, and microgrids. DC-DC converters are categorized into isolated and non-isolated types based on the degree of electrical isolation between input and output. Isolated converters utilize transformers to decouple the source and load, enhancing operational safety but increasing cost and device footprint. Additionally, transformer leakage inductance can induce voltage spikes, leading to stability challenges [3], [4]. Conversely, non-isolated converters are widely favored due to their superior efficiency, compact form factor, cost-effectiveness, and minimal input current ripple. These attributes make them particularly suitable for low-power applications requiring a simple design and high economic viability [5], [6].

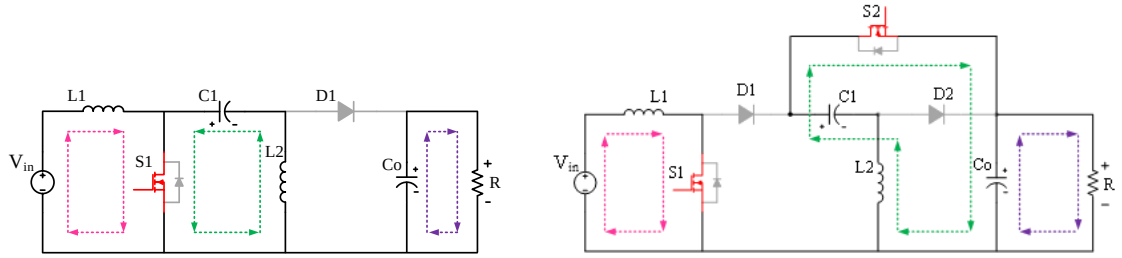


Fig. 1. (a) Current stress on the power switch (S1) in the SEPIC converter; (b) Operation of the structure under reduced current stress.

Standard non-isolated DC-DC converter topologies used in voltage step-up and step-down applications include buck, boost, buck-boost, SEPIC, Ćuk, Zeta, and flyback converters. Renewable energy sources like solar, wind, and biomass exhibit fluctuating output power, leading to unstable voltage levels and complicating grid-connected inverter operations. Therefore, converters must be capable of dynamic voltage regulation, maintaining low ripple levels while alleviating stress on semiconductor components [7]. Among these options, SEPIC is often preferred over flyback because it maintains an output voltage with the same polarity as the input while producing lower ripple currents.

In DC-DC converters and power semiconductor devices, current and voltage stress are key parameters that directly influence efficiency, reliability, and operational lifetime.

These stresses are the maximum current and voltage applied to or passing through the device. Specifically, the maximum current stress occurs in DC-DC converters when the switch is in conduction. In contrast, the maximum voltage stress is observed across the semiconductor in the off state.

The conventional SEPIC converter exhibits a relatively low voltage gain and suffers from a significant drawback: during the conduction interval, switch S1 simultaneously carries the current from inductor L1 and capacitor C2. This condition imposes excessive current stress on the switch, leading to higher conduction losses, increased thermal dissipation, reduced efficiency, and shortened lifetime.

An improved SEPIC configuration introduces an additional diode D1 and switch S2 to alleviate this limitation while enhancing the voltage gain. In this arrangement, when S1 and S2 are turned on, switch S1 conducts only the current I_{L1}, whereas I_{L2} is delivered through S2 to the load. As a result, S1 is subjected to a single current path during conduction. Beyond reducing current stress, the proposed modification achieves a higher voltage gain than the conventional SEPIC converter. A detailed analysis and verification of the reduced current and voltage stresses are presented in Section 2.

This study proposes a novel buck-boost configuration to address this challenge by restructuring the circuit with an additional switch and diode to reroute the capacitor C1 current away from switch S1. This modification substantially mitigates the stress on S1, enhancing efficiency and reliability.

2. Proposed topology

2.1. Proposed converter topology

Several strategies can be employed to mitigate the issue of excessive current stress on switches and diodes in SEPIC converters, such as increasing the current rating of these components or implementing parallel configurations to share the current load. However, upgrading the current rating significantly raises costs, as high-current-rated switches and diodes are considerably more expensive than their lower-rated counterparts. Additionally, as shown in Fig. 2, incorporating a parallel switch to alleviate current stress on the main power switch remains feasible. However, synchronizing both switches to conduct simultaneously is far from straightforward. The current distribution between the two switches primarily depends on their internal resistance, and since each component has a unique resistance value, achieving an optimal current balance poses a significant challenge. This requires intricate PCB design techniques and substantial resource consumption. Consequently, the efficiency of using two parallel switches falls short compared to employing two independently positioned switches.

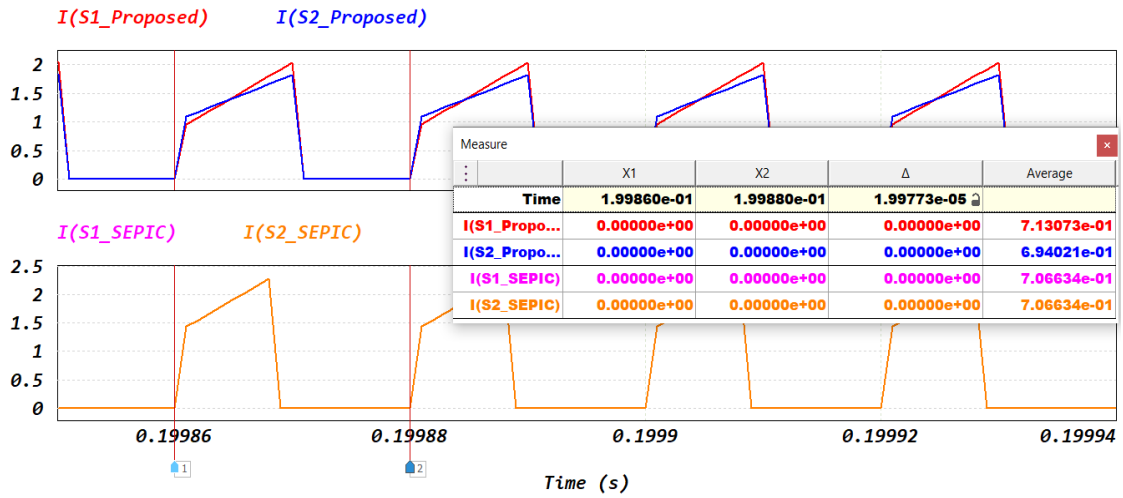


Fig. 2. Comparison of the current through the semiconductor switch of the SEPIC configuration with an additional parallel-connected switch and the proposed configuration.

To overcome these limitations, this study introduces an innovative configuration, illustrated in Fig. 3, by restructuring the SEPIC converter. The proposed design integrates an additional diode (D1) to block the capacitor C1 current from flowing through switch S1 while incorporating a secondary switch S2 to redirect this current toward inductor L2. As a result, current stress on both the switches and diodes is significantly reduced, enhancing overall system efficiency and reliability.

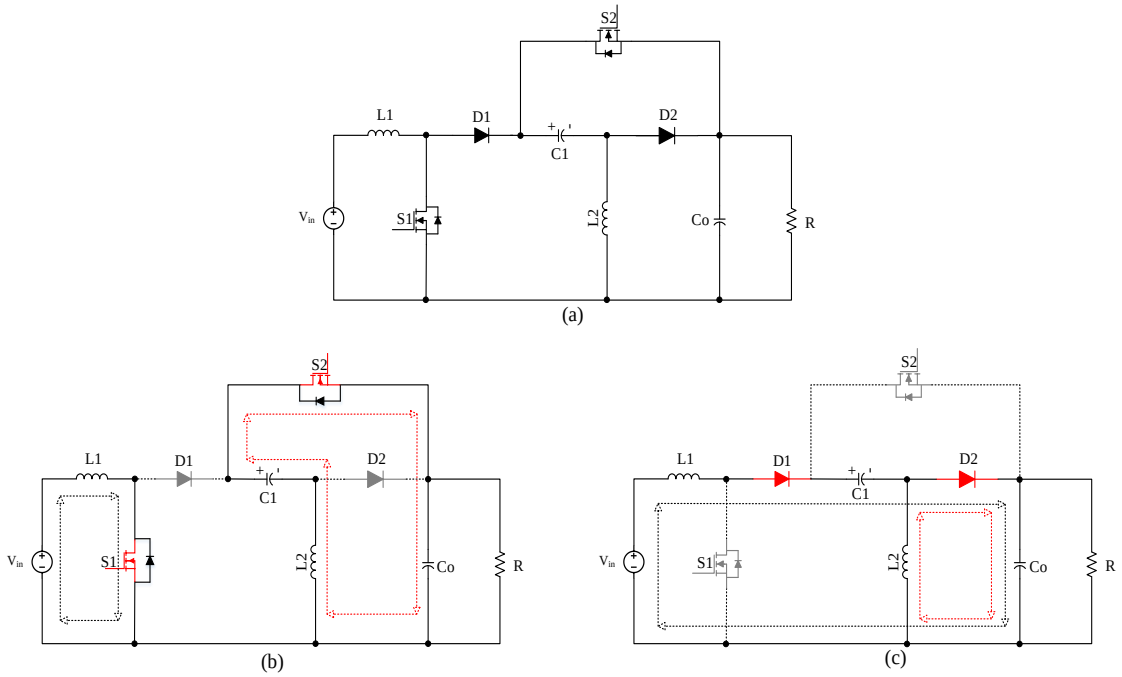


Fig. 3. (a) Proposed converter, (b) Operating stage 1, (c) Operating stage 2.

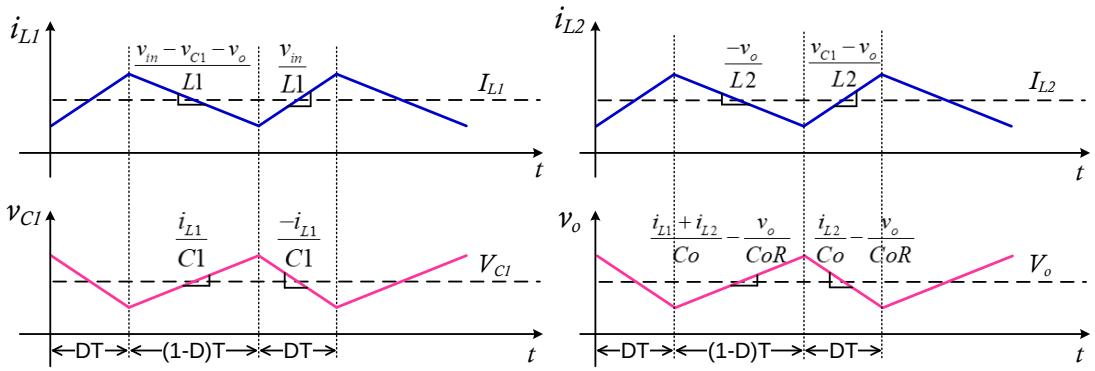


Fig. 4. Typical waveforms of the proposed converter in the time domain.

The proposed converter, as illustrated in Fig. 3a, operates at a switching frequency of 50 kHz. The semiconductor switches S1 and S2 are synchronously controlled to turn on and off, while diodes D1 and D2 remain consistently reverse-biased throughout the switching cycle.

This converter functions primarily in two operating modes, assuming that the inductors and capacitors are designed with sufficiently large values to ensure continuous conduction mode (CCM). Under these conditions, the voltages across capacitors C1 and Co remain stable. Notably, the inductor L1 maintains a steady input current across both operating modes, effectively minimizing input current fluctuations. Simultaneously, the current through inductor L2 ensures continuous output current delivery, enhancing power quality. A detailed analysis of the two operating modes will be presented in Section 2.2.

2.2. Operating mode

The switches S1 and S2 remain active for a duration corresponding to the duty cycle DT, as illustrated in Figs. 3b and 4. During this interval, diodes D1 and D2 stay reverse-biased, preventing current conduction. At this stage, the input voltage V_{in} energizes inductor L1, while capacitor C1 supplies energy to inductor L2. The voltage across capacitor C1 is identical to the voltage imposed on diode D2, representing the stress level that this diode must endure. Likewise, the output voltage V_o reflects the voltage stress experienced by diode D1.

During the interval (1-D)T, as illustrated in Figs. 3c and 4, switches S1 and S2 are turned off, which allows diodes D1 and D2 to become forward-biased and conduct current. At this stage, the input voltage V_{in} and the energy previously stored in inductor L1 recharge capacitor C1 through diodes D1 and D2. At the same time, inductor L2 delivers its stored energy to the output capacitor Co via diode D2. Here, D denotes the duty cycle, defined as the ratio between the switch-on time and the total switching period

T. Therefore, the interval (1-D)T represents the off-time of the switches, during which the passive components release energy to maintain the output voltage.

The differential equations governing the relationships between voltage and current during the DT and (1-D)T intervals can be derived and are expressed in (1)

$$\begin{cases} L2\dfrac{di_{L2}}{dt} = Dv_{in} + (1-D)(v_{in} - v_{C1} - v_o) \\ L2\dfrac{di_{L2}}{dt} = D(v_{C1} - v_o) + (1-D)(-v_o) \\ C1\dfrac{dv_{C1}}{dt} = D(-i_{L2}) + (1-D)(i_{L1}) \\ Co\dfrac{dv_o}{dt} = D\left(i_{L2} - \dfrac{v_o}{R}\right) + (1-D)\left(i_{L1} + i_{L2} - \dfrac{v_o}{R}\right) \end{cases} \quad (1)$$

2.3. Voltage conversion ratio

In a steady-state condition, inductors can be regarded as elements with zero reactance, meaning the average voltage across them over a working cycle is zero. By applying the Volt-second balance principle from (1), the relationship between the voltage and current parameters within the system can be derived and expressed, as shown in (2)

$$\begin{cases} DV_{in} + (1-D)(V_{in} - V_{C1} - V_o) = 0 \\ D(V_{C1} - V_o) + (1-D)(-V_o) = 0 \end{cases} \quad (2)$$

Based on (2), the voltages across capacitors C1 and Co are derived as shown in (3) and (4), respectively.

$$V_{C1} = \frac{V_{in}}{1-D^2} \quad (3)$$

$$V_o = \frac{DV_{in}}{1-D^2} \quad (4)$$

Hence, the voltage conversion ratio (M) of the proposed converter can be expressed and determined using (5)

$$M = \frac{V_o}{V_{in}} = \frac{D}{1-D^2} \quad (5)$$

2.4. Voltage and current stress

The voltage stress on the switches, defined as their maximum operating voltage, is determined by Eqs. (6)-(12):

$$V_{S1} = \frac{(1+D)V_{in}}{1-D^2} \tag{6}$$

$$V_{D1} = \frac{DV_{in}}{1-D^2} \tag{7}$$

$$V_{S2} = V_{D2} = \frac{V_{in}}{1-D^2} \tag{8}$$

The average current through power switch S1 can be determined as given in Eq. (9)

$$I_{S1} = \frac{D^2}{1-D^2} I_{in} \tag{9}$$

The average current through diode D1 can be determined by Eq. (10)

$$I_{D1} = \frac{D}{1+D} I_{in} \tag{10}$$

The average current through power switch S2 can be determined as given in Eq. (11)

$$I_{S2} = \frac{DI_{in}}{1+D} \tag{11}$$

The current through switch D2 can be determined using Eq. (12)

$$I_{D2} = \frac{I_{in}}{1+D} \tag{12}$$

3. Simulation results

This article conducts a detailed analysis to assess the proposed converter's performance. It compares its current handling capabilities with other standard buck-boost configurations, including the SEPIC converter and designs described in previous studies [8], [9]. The analysis focuses on energy efficiency and factors related to stability and reliability during operation.

Additionally, circuit components are numbered in the order of their appearance to facilitate observation and verification in simulations. Ideal component models available in the PSIM software are utilized, making it easier to track and identify each component in the system, as illustrated in Fig. 5. A 48 VDC power supply is used as the test input to ensure objectivity and consistency in the measurements. Table 1 provides a detailed overview of the simulation parameters and converter settings while illustrating the relationship between the total circuit components and the resulting voltage gain. This experimental setup ensures equivalent conditions, providing a solid foundation for accurate evaluation and fair performance comparison of the converter configurations.

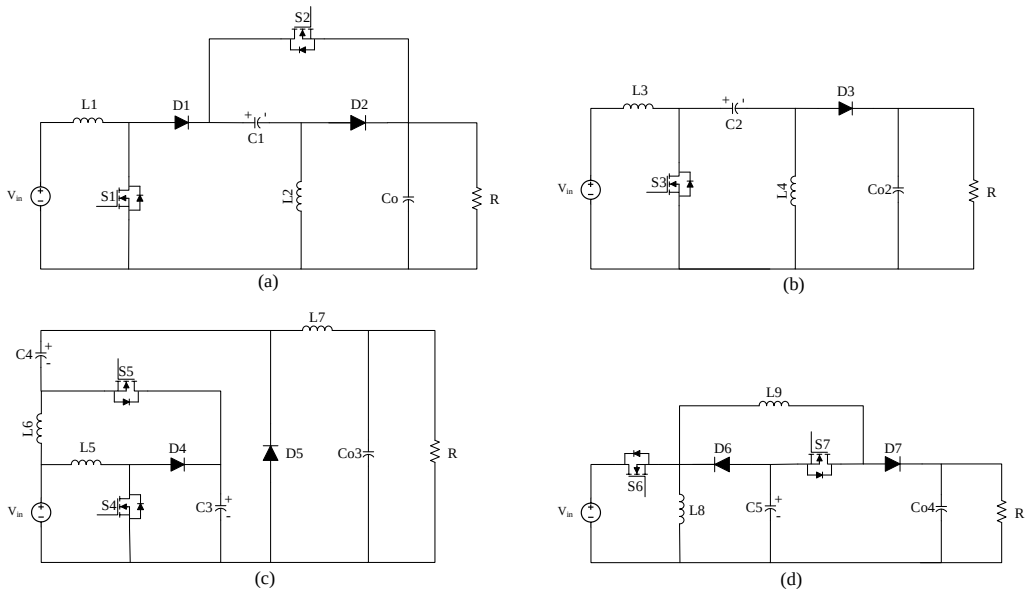


Fig. 5. (a) Proposed converter, (b) SEPIC converter, (c) Converter according to study [8], (d) Converter according to study [9].

Tab. 1. Setting parameters of the converters

Components	Proposed		SEPIC		[8]		[9]	
	Symbol	**Value**	**Symbol**	**Value**	**Symbol**	**Value**	**Symbol**	**Value**
Switch	S1, S2	Default in PSIM	S3	Default in PSIM	S4, S5	Default in PSIM	S6, S7	Default in PSIM
Diode	D1, D2	Default in PSIM	D3	Default in PSIM	D4, D5	Default in PSIM	D6, D7	Default in PSIM
Capacitor	C1, Co1	47 uF, 100 uF	C2, Co2	47 uF, 100 uF	C3, C4, Co3	47 uF, 100 uF	C5, Co4	47 uF, 100 uF
Inductor	L1, L2	0.4 mH	L3, L4	0.4 mH	L5, L6, L7	0.4 mH	L8, L9	0.4 mH
Load	R	15 Ω	R	15 Ω	R	15 Ω	R	15 Ω
Source	V_{in}	48 V	V_{in}	48 V	V_{in}	48 V	V_{in}	48 V
Total	8		6		10		8	
Voltage gain	$\frac{D}{1-D^2}$		$\frac{D}{1-D}$		$\left(\frac{D}{1-D}\right)^2$		$\left(\frac{D}{1-D}\right)^2$	

Switching frequency: 50 kHz
Voltage gain with buck mode experiment: M = 0.66
Voltage gain with boost mode experiment: M = 2

Table 1 shows that the proposed converter has the same total number of components as the converter from the study in [9] across all elements, resulting in a comparable investment cost between the two. Among all the referenced converters, the one in the study [8] has the highest investment cost. However, compared to the SEPIC converter,

the proposed converter includes one additional switch and one diode. In practice, to reduce current stress on the switches and diodes in the SEPIC converter, the current rating of the switches can be doubled, reducing the PCB size. However, switches with higher current ratings come at a significantly higher cost. Alternatively, another solution is to use two parallel switches with the same current rating. In this case, the component count of both circuits is nearly identical, resulting in minimal investment cost differences.

3.1. Current stress on the switches and diodes in the buck mode

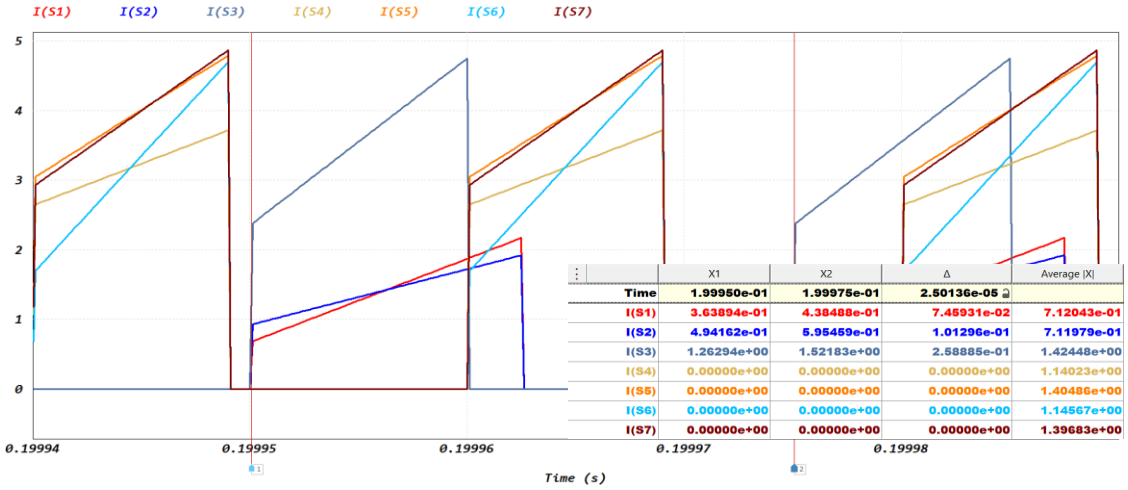


Fig. 6. Current through the switches of the converters in buck mode.

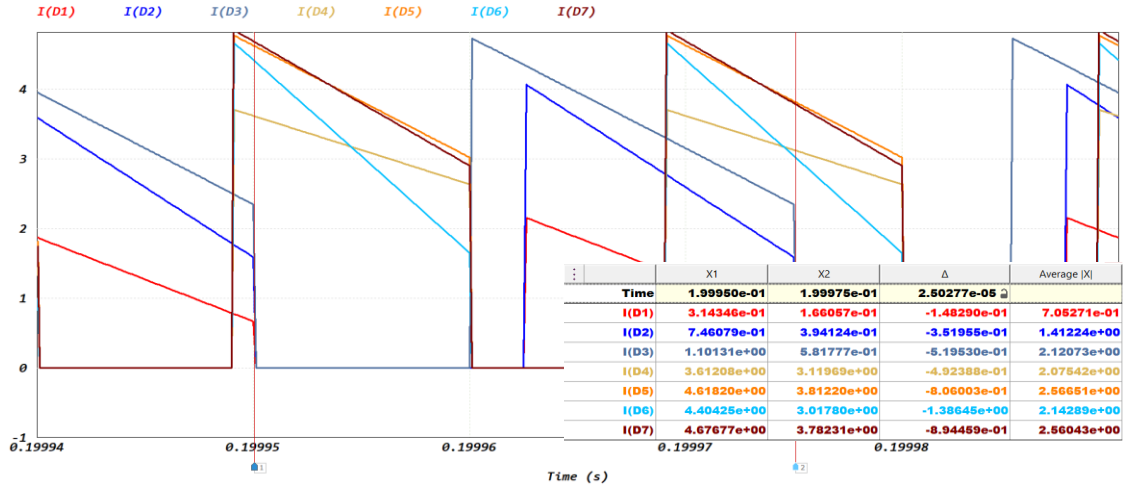


Fig. 7. Current through the diodes of the converters in the buck mode.

The current waveforms through the switches of the converter operating in buck mode are illustrated in Fig. 6, with a voltage conversion ratio of M = 0.66 (corresponding to an output voltage of 32 VDC). The proposed converter demonstrates exceptional efficiency, with the average current through switches S1 and S2 reaching 0.71 A,

representing 50.93% of the input current under ideal conditions. In contrast, the SEPIC converter exhibits an average current of 1.42 A through switch S3, accounting for the highest percentage of 101.87%. For the two-stage converter discussed in the study [8], the average current through switch S4 is similar to that through switch S6 in the converter presented in [9], with a ratio of 81.78%. Similarly, the average current through switches S5 and S7 in these two converters is approximately 1.4 A, representing 100.43% of the total current. In summary, in buck mode, the proposed converter exhibits a significantly reduced current stress across the switches, leading to higher operational efficiency and contributing to the extended lifespan of the semiconductor switches.

Figure 7 illustrates the current through the diodes in the converter configuration. The average current through diode D1 in the proposed converter is 0.7 A. Meanwhile, the current through diode D2, influenced by the currents in inductors L1 and L2 during phase 2, is relatively higher, with an average value of 1.41 A. Compared to other converters, the current through diode D2 in the proposed converter is approximately 55% lower than the peak current observed through diodes D5 and D7 in studies [8] and [9]. In these studies, the average current through diodes D4 and D6 are 2.07 A and 2.14 A, respectively.

3.2. Current stress on the switches and diodes in the boost mode

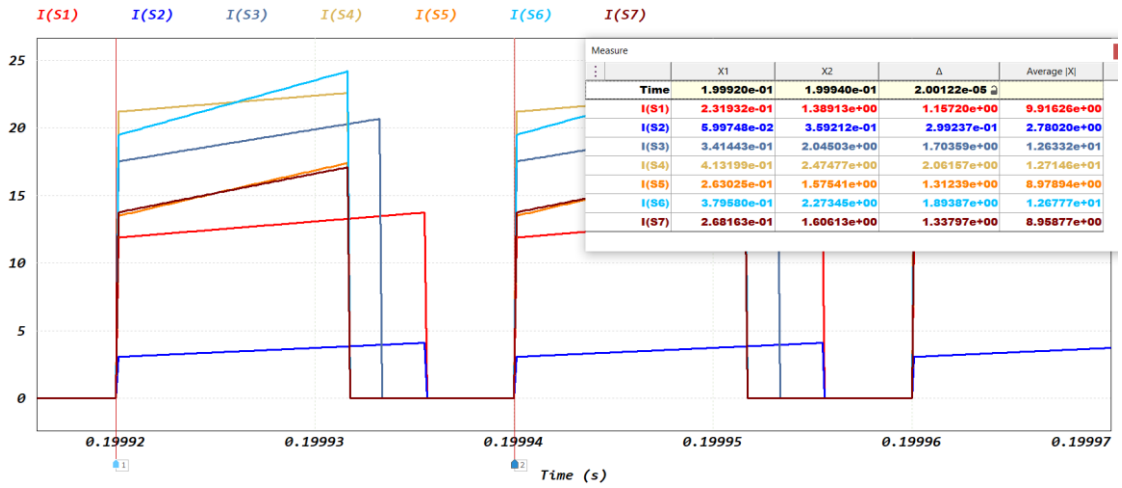


Fig. 8. Current through the switches of the converters in the boost mode.

With a voltage conversion ratio of M = 2, used as the test model for the boost mode, Fig. 8 illustrates the current waveforms through the converter switches. For the proposed converter, the average current through switches S1 and S2 are 9.91 A and 2.78 A, respectively, accounting for 77.42% and 21.72% of the ideal input current. In contrast, the SEPIC converter shows the highest average current through switch S3, reaching 12.63 A, representing 98.67% of the ideal input current. The average current through switch S4

of the converter in [8] is nearly equivalent to the current through switch S6 of the two-stage converter in [9], with a ratio of 99.29%. Similarly, the average current through switches S5 and S7 in these two converters is approximately 8.97 A, corresponding to 70.07% of the ideal input current.

The proposed converter demonstrates significantly lower current stress through switch S2 in boost mode. However, this converter is better suited for step-down applications due to its characteristic structure with a first-order term in the denominator. When operating in boost mode, switch S1 needs to remain active longer than other converters, resulting in a 7.35% higher current through S1 compared to the current through switches S5 and S7 in the studies [8], [9].

Figure 9 illustrates the current through the diodes in the converter configuration. For the proposed converter, the average current through diode D1 is 2.9 A, while the current through diode D2 reaches 3.71 A. Compared to other converters, the current through diode D2 in the proposed converter is approximately 40.45% lower than the peak current observed through diodes D4 and D6 [8]. The average current through diodes D5 [8] and D7 [9] is approximately 6.46 A.

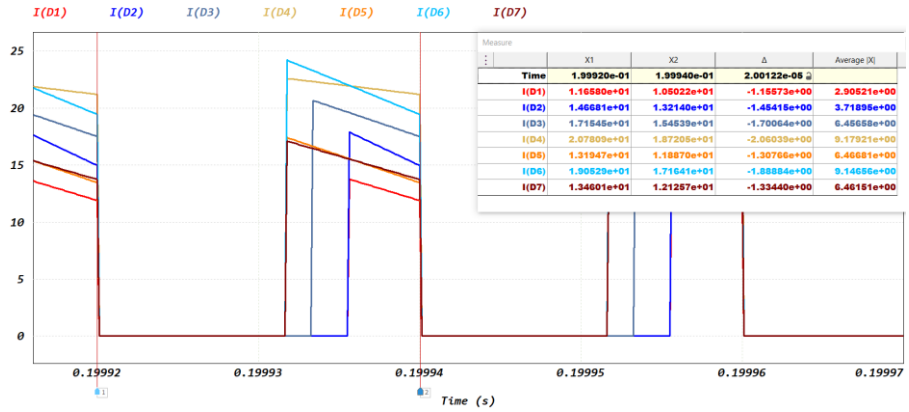


Fig. 9. Current through the diodes of the converters in the boost mode.

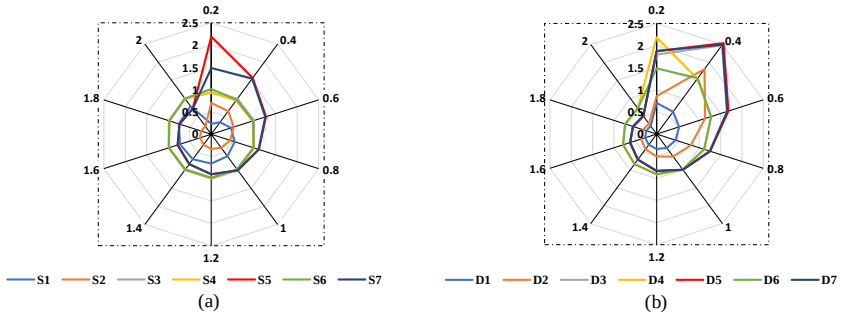


Fig. 10. Current through the diodes of the converters in the boost mode.

Figures 10a and 10b present the simulation results for the current overload factor under ideal conditions for the switches and diodes across a range of voltage conversion ratios from 0.2 to 2. The results indicate that the proposed converter maintains the current through switch S2 at no more than 0.7 times the source current, while the current through switch S1 peaks at only 0.77 times the source current. The current through diode D1 reaches 70% of the source current, while the current through D2 exceeds 81%. These values are significantly lower than the SEPIC converter and the converters investigated in [8], [9]. These findings validate the converter's exceptional capability in optimizing current stress, contributing to improved operational efficiency and extended system lifespan.

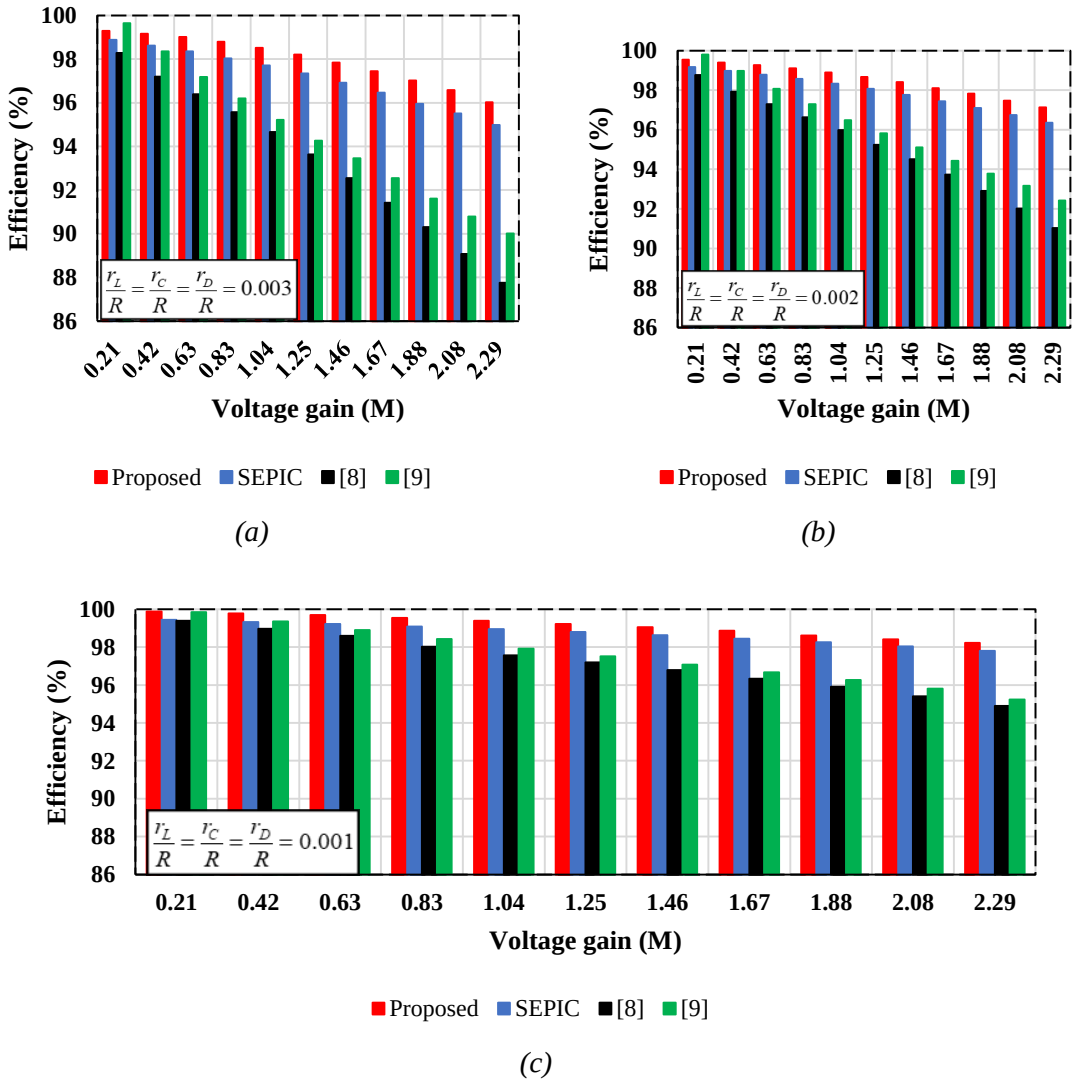


Fig. 11. Efficiency of the converters with parasitic resistance proportional to the load value: (a) 0.003, (b) 0.002, (c) 0.001.

To comprehensively assess the proposed converter's performance and operational stability range, an experiment was conducted by simulating parasitic resistance across critical components such as inductors, capacitors, and diodes. In this experiment, parasitic resistances were applied at ratios of 0.001, 0.002, and 0.003 relative to the load resistance. This approach not only facilitates the overall efficiency evaluation but also identifies the impact of parasitic factors on the converter's stability and operational capabilities under various conditions, thereby providing valuable insights into potential challenges. As a result, the operational effectiveness of the converter in real-world environments was thoroughly validated. The converter's parameters were consistently configured to maintain objectivity throughout the evaluation.

Figure 11 clearly illustrates the effect of parasitic resistance on the converter's efficiency. Specifically, in Fig. 11a, with a parasitic resistance ratio of 0.003 relative to the load resistance, the secondary converter [8] achieves a maximum efficiency of only 98.28%, operating stably within the voltage conversion ratio range of 0.2 to 2.29, the lowest among the converters analyzed. The converter from the study [9] performs better, with a peak efficiency of 99.64%. However, it rapidly loses its advantage, dropping its efficiency below the proposed converter within the voltage ratio range of 0.4 to 2.29. In contrast, the proposed converter and the SEPIC converter maintain stable operation across a broader range, with the proposed converter reaching a peak efficiency of 99.29%.

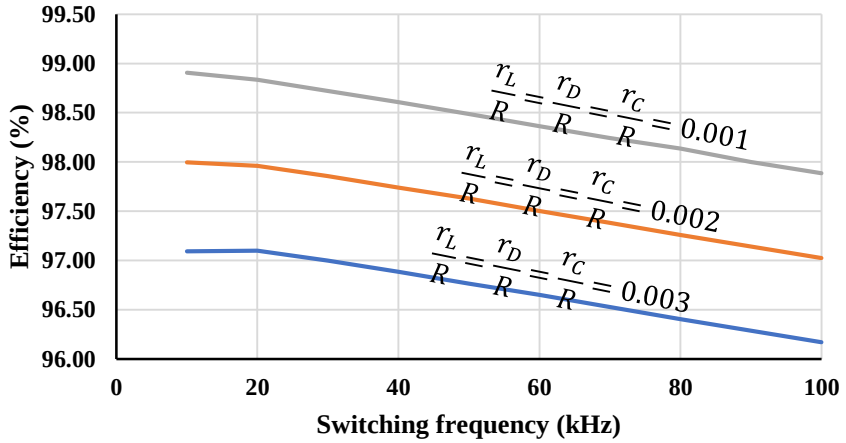
Figure 11b further substantiates the advantages of the proposed converter, with an efficiency of 99.54%, surpassing the SEPIC converter by 0.38% and the converter in [8] by 0.78%, even though these configurations also improve their operational stability range. The converter configuration in the study [9] initially outperforms, achieving an efficiency of up to 99.79%. However, it rapidly deteriorates and becomes less stable than the proposed converter.

Finally, Fig. 11c reveals that when the effect of parasitic resistance is minimized, the efficiency of all converters exceeds 94%. However, the proposed converter continues to lead with an impressive efficiency of 99.88%, demonstrating exceptional performance in minimizing losses and optimizing overall efficiency.

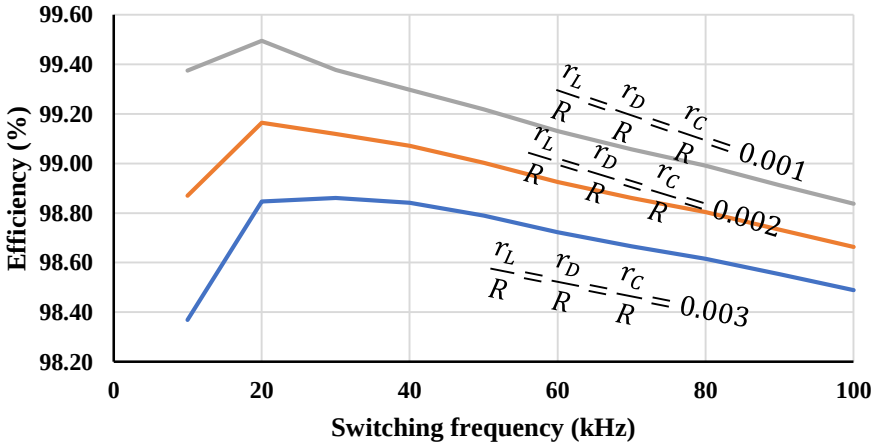
An experiment was conducted in step-up and step-down modes to assess the converter’s efficiency across switching frequencies. In the step-up mode, to ensure objectivity, the internal resistances of the components were added with values of 0.001, 0.002, and 0.003 times the load resistance. The experimental parameters were maintained as described in Tab. 1.

Based on Figs. 12a and 12b, it can be observed that a switching frequency of

20 kHz provides optimal efficiency for most of the experiments. However, the difference is negligible when comparing the efficiency between the two frequencies of 20 kHz and 50 kHz under the same operating conditions (< 1%). At the same time, the cost of increasing the inductance and capacitance values is relatively high. Moreover, a higher switching frequency helps reduce ripple in both current and voltage within the converter. Nonetheless, if the frequency is too high, the microcontroller will require a larger counter, making implementation more challenging. Therefore, this study has opted for a switching frequency of 50 kHz to ensure compatibility with widely used microcontrollers, such as Arduino, thus facilitating future experiments.



(a)



(b)

Fig. 12. The efficiency of the proposed converter with respect to frequency under operating conditions: (a) Boost mode (M = 2), (b) Buck mode (M = 0.2).

3.3. Simulation with a DC motor load

Table 2 presents the technical specifications of the two experimental configurations when the load is a DC motor exhibiting nonlinear current characteristics. In the simulation study, the component parameters are identical across both configurations to ensure objectivity and fairness when evaluating their performance. The DC motor selected as the load has the parameters listed in Tab. 2, and it operates under a varying torque profile: from 0 to 1 second, the torque remains constant at 1 N·m; at 1 second, the load abruptly shifts to 25 N·m and continues at this level until the end of the simulation at 2 seconds. The detailed experimental setup is illustrated in Fig. 13.

Figure 15 highlights the pronounced difference in output voltage quality between the two topologies. Specifically, the proposed converter exhibits an output voltage ripple of only 0.127 V, whereas the SEPIC configuration records a ripple as high as 2.42 V under a load torque of 1 N·m. This corresponds to a reduction by nearly a factor of 19, indicating the superior capability of the proposed structure in suppressing disturbances and maintaining voltage stability. When the load torque increases to 25 N·m, although the output voltage ripple of both converters rises, the proposed topology still preserves a clear advantage, with a ripple amplitude approximately 3.9 times lower than that of the SEPIC, thereby demonstrating robust stability even under heavy load conditions.

Tab. 2. Simulation specifications under DC motor load conditions

Components	**Proposed**		**SEPIC**	
	Symbol	**Value**	**Symbol**	**Value**
Switch	S1, S2	Default in PSIM	S3	Default in PSIM
Diode	D1, D2	Default in PSIM	D3	Default in PSIM
Capacitor	C1, Co1	47 uF, 100 uF	C2, Co2	47 uF, 100 uF
Inductor	L1, L2	0.4 mH	L3, L4	0.4 mH
Load	DC Machine	Ra = 3.1 Ω La = 0.024 H Rf = 75 Ω Lf = 0.5 H Vt = 100 V Ia = 92.6 A N = 1500 rpm If = 1.33 A	DC Machine	Ra = 3.1 Ω La = 0.024 H Rf = 75 Ω Lf = 0.5 H Vt = 100 V Ia = 92.6 A N = 1500 rpm If = 1.33 A
Source	V_{in}	48 V	V_{in1}	48 V
Total	8		6	
Voltage Gain	$\frac{D}{1-D^2}$		$\frac{D}{1-D}$	
Note	Switching frequency: 50 kHz Voltage gain simulation: M = 2			

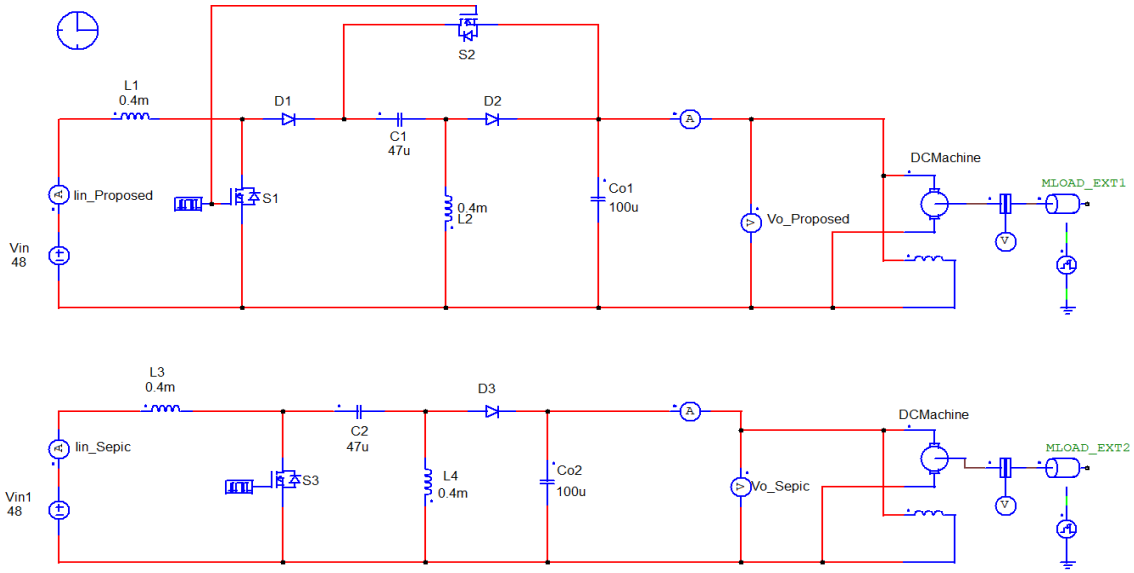


Fig. 13. Simulation schematic for comparing the stability of the proposed converter and the SEPIC configuration under a DC motor load.

Simulation results with a DC motor load, where the input current varies with load torque, confirm that the proposed converter sustains significantly better voltage and current stability and achieves higher efficiency compared to the SEPIC, despite delivering the same output power to the load. This benefit is primarily achieved through a lower input current, coupled with markedly reduced voltage ripple and current oscillations at both input and output.

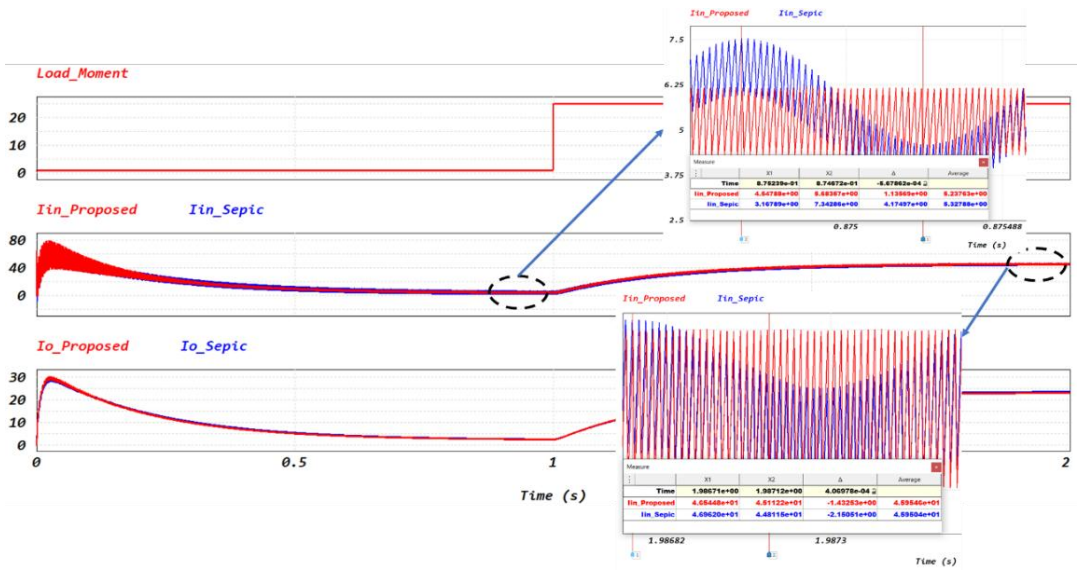


Fig. 14. Input current waveforms of the proposed converter and the SEPIC converter under varying load torque.

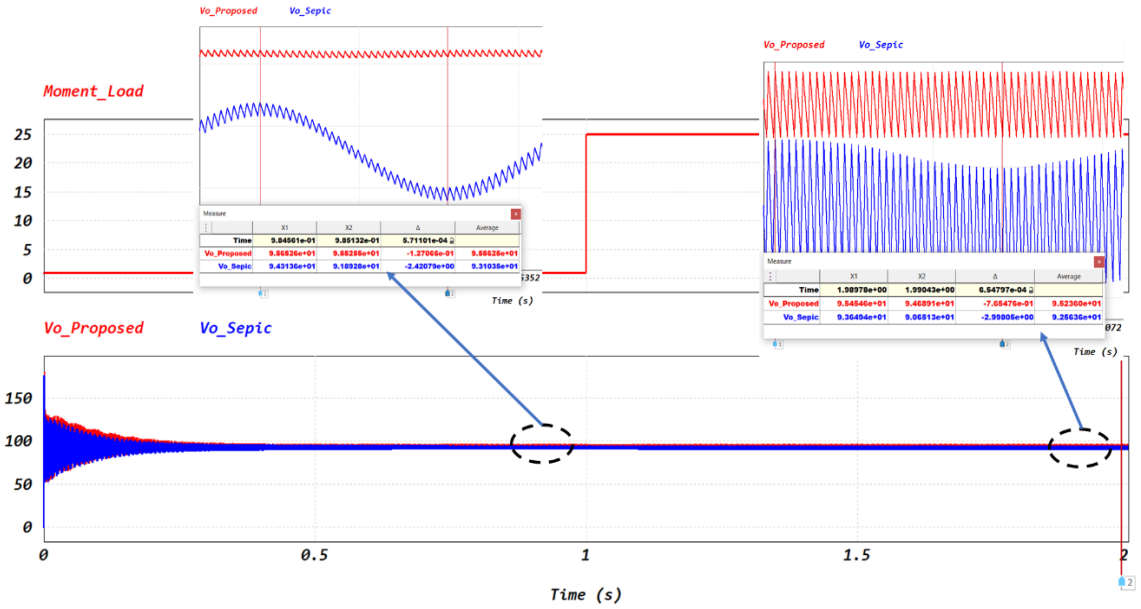


Fig. 15. Output voltage waveforms versus load torque of the proposed converter and the SEPIC converter.

The underlying cause of this performance gap stems from each topology's distinct energy transfer mechanisms. In the SEPIC converter, energy from the source must pass through a series of elements including the coupling capacitor C1, the semiconductor switch S1, and the inductor L2- before reaching the load. This indirect transfer path not only lengthens the energy delivery route, leading to greater delay and losses, but also results in a discontinuous supply to the load due to the charge–discharge dynamics of the coupling capacitor. Such discontinuity is the primary reason for the large voltage ripple and unstable output current. Moreover, the additional conduction through multiple passive and switching devices introduces higher conduction and switching losses, further reducing overall efficiency.

In contrast, the proposed converter incorporates a refined circuit structure that allows the load to draw energy directly from both the source and the inductor during both operating states of the semiconductor switch. This ensures a continuous current supply to the load, effectively minimizing instantaneous interruptions, smoothing current characteristics, and substantially reducing output voltage ripple. Furthermore, by eliminating the intermediate energy transfer stage through the coupling capacitor, the power transfer path is shortened, losses are reduced, and efficiency is enhanced. Most

importantly, this direct energy delivery mechanism enables the system to respond rapidly to sudden changes in load torque, thereby maintaining superior dynamic stability.

Through these structural enhancements and optimized energy transfer principles, the proposed converter not only achieves higher voltage and current stability but also delivers outstanding energy efficiency, effectively overcoming the inherent limitations of the SEPIC configuration.

4. Conclusion

The proposed converter exhibits superior performance with significantly reduced current stress on semiconductor components. In buck mode (M = 0.66, V_o = 32 VDC), the average current through S1 and S2 reaches 0.71 A (50.93% of the input current), substantially lower than that of the SEPIC converter (1.42 A, 101.87%). In boost mode (M = 2), the current through S1 peaks at 9.91 A (77.42%), while S2 carries only 2.78 A (21.72%), marking a notable reduction compared to SEPIC (12.63 A, 98.67%).

The converter maintains high efficiency even under parasitic resistance conditions, achieving a peak efficiency of 99.29%, surpassing the secondary converter in [8] (98.28%) and only slightly trailing the design in [9] (99.64%). When parasitic effects are minimized, efficiency improves further to 99.88%. Regarding switching frequency, although the performance variation between 20 kHz and 50 kHz remains marginal (< 1%), the latter is selected to strike a balance between efficiency, ripple suppression, and compatibility with widely used microcontrollers. These findings underscore the converter's capability to optimize current distribution, enhance operational efficiency, and extend system longevity. As a result of the enhanced switch–diode structure, the proposed converter delivers energy to the load during both switching states. In contrast, the SEPIC must transfer energy sequentially through the capacitor and inductor. Consequently, this direct path ensures continuous current supply, lower ripple, and higher efficiency under nonlinear DC motor load conditions.

Acknowledgement

This work is supported by the Electrical and Renewable Energy Systems Laboratory (C201), the Industrial Power System Control Laboratory (C402) at the Ho Chi Minh City University of Technology and Engineering.

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BỘ CHUYỂN ĐỔI SEPIC CẢI TIẾN GIÚP GIẢM ÁP LỰC DÒNG ĐIỆN ĐẶT TRÊN CÁC THIẾT BỊ CHUYỂN MẠCH VÀ ĐI-ỐT TRONG KHI VẪN DUY TRÌ HIỆU SUẤT CAO

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Tóm tắt: Bài báo trình bày một thiết kế bộ chuyển đổi DC buck-boost cải tiến giúp giảm thiểu dòng điện chuyển mạch vốn có trong các bộ chuyển đổi SEPIC. Nghiên cứu cho thấy bộ chuyển đổi đề xuất làm giảm đáng kể dòng điện qua các thiết bị chuyển mạch và đi-ốt trong quá trình chuyển mạch. Nghiên cứu đã thực hiện các phân tích ở trạng thái xác lập, bao gồm độ lợi chuyển đổi điện áp, hiệu suất và dòng điện trên các phần tử chính của bộ chuyển đổi. Ngoài ra, các thí nghiệm mô phỏng kết hợp với quá trình đánh giá lý thuyết cũng được thực hiện trong chế độ giảm áp và tăng áp, tải động cơ một chiều với mô men thay đổi. Kết quả cho thấy bộ chuyển đổi đề xuất giảm được dòng điện qua các khóa bán dẫn và đi-ốt S1, S2, D1 và D2, trong khoảng độ lợi điện áp thay đổi từ 0,2 đến 2. Kết quả khi so sánh với bộ chuyển đổi SEPIC và các cấu hình khác đã được phân tích, cho thấy bộ chuyển đổi này có hiệu suất cao hơn và tổn thất công suất thấp hơn, điện áp ngõ ra ổn định hơn. Hơn nữa, thí nghiệm cũng xem xét đến sự ảnh hưởng của các điện trở ký sinh trên các phần tử chính, kết quả cho thấy bộ chuyển đổi đề xuất có hiệu suất cao hơn các giải pháp hiện tại bằng cách giảm thiểu dòng điện qua các phần tử chính, do đó sẽ nâng cao độ tin cậy, giảm thiểu tổn thất công suất qua các linh kiện chuyển mạch, qua đó cho thấy bộ chuyển đổi đề xuất là lựa chọn tốt cho các ứng dụng cần sự thay đổi điện áp một cách linh hoạt.

Từ khóa: *Bộ chuyển đổi tăng-giảm áp; bộ chuyển đổi SEPIC; không cách ly; độ lợi điện áp; đầu ra dương.*

Received: 23/04/2025; Revised: 23/09/2025; Accepted for publication: 27/01/2026

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