FPGA IMPLEMENTATION OF HIGH-PERFORMANCE DOA ESTIMATION USING A UNIFORM CIRCULAR ARRAY

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Abstract

In this paper, the author presents a signal processing hardware architecture that locks the frequencies of signals of interest present at the input, tracks them if their frequency changes and estimates the direction-of-arrival (DOA) of the interest signals using a uniform circular array. The proposed hardware architecture is described in detail, implemented and verified by practical experiments on FPGA chip. Experimental results show that the DOA estimation accuracy is smaller than 1 degree. This DOA estimation accuracy is suitable for electronic attack systems.

Keywords: *Direction-of-Arrival (DOA); digital down converter (DDC); frequency tracker; correlation interferometer; uniform circular array (UCA).*

1. Introduction

The direction of Arrival (DOA) is one of the crucial parameters in both civilian and defense monitoring applications. In defense applications (radar, sonar, radio-electronic warfare, etc.), DOA techniques have been applied for air traffic control, target acquisition, position location and tracking systems. Also, in civilian applications, DOA techniques can be used in wireless communication monitoring for localization of mobile terminals. DOA estimation is an important task in smart (phased array) antennas for wireless communications. DOA estimation methods can be used to design and adapt the directionality of smart antennas, i.e. increase spatio-temporal filtering capability that is needed in spatio-temporal signal separation and interference suppression. The smart antennas can provide better performance in increasing the signal to noise ratio (SNR) for each mobile user and increasing the effective range, and allow for multiplexing co-channel users.

DOA estimation techniques have been tackled by a wide range of different methods, and can be classified into categories: correlation-based, spectrum-based and parametric estimation methods. The spectrum-based methods, such as beamforming techniques [1], subspace-based techniques [2-7] and spatial smoothing for correlated and coherent signals [8], and the parametric estimation methods, including Maximum Likelihood Estimation [9] and subspace fitting algorithms [10], provide high-resolution

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DOA estimates. However, these algorithms involve a large number of complex-valued computations because of the eigenvalue decomposition of the complex covariance matrix and spatial spectrum peak search. Therefore, the hardware implementations of the spectrum-based algorithms are complex. Moreover, the spectral peak search occupies some of the most time in the subspace category and class of subspace fitting algorithm that may be cannot guarantee the real-time signal processing requirements. Most DOA estimation algorithms are mainly evaluated using software simulations. In addition to the dominant peaks, there are many other small peaks in the computed spatial spectrum. Therefore, it's difficult to search the number and location of signal sources from dominant peaks by using only analytical methods. In practice, it is needed to estimate the number of sources from the received signal that is the most demanding in terms of computational complexity.

The correlation-based methods (correlation interferometer) [11] are widely applied due to the advantages of high DOA estimation accuracy, simple algorithm and flexibility. The interferometers get the space phase differences between receiving antenna elements. The DOA angles can be found from correlation function. The correlation interferometers are developed for a single source. In practice, there are generally more than one incoming signal sources. In this case, multichannel structures of interferometers can be used to estimate the incoming directions of signal in each channel.

Among direction finding techniques, DOA estimation error is a function of the SNR and number of antenna elements. With a purpose to improve the performance of the DOA estimation, this paper introduces a signal processing hardware architecture of a DOA estimation receiver including a frequency tracker, DDCs and correlation interferometer. The DDCs are used to filter the unwanted spectrum outside of the band of interest that increases SNR. The frequency tracker includes fast Fourier transform (FFT) and weighted frequency tracking unit to be used to analyze unknown signals, locates a window of frequency samples with the specified size to calculate which frequency to track. This frequency tracker is very well suitable to frequency detection of the frequency hopping communication systems [12].

The remainder of this paper is organized as follows: Section 2 gives parametric data model of multiple RF (radio frequency) sources and shows signal model with one source in the special case. Section 3 describes the proposed hardware scheme on FPGA. The experimental results are proved in section 4. Finally, Section 5 concludes the paper.

Let us define the notations used in this paper. Samples in the time and frequency domain are denoted by lower-case and upper-case letters with an index n and k,

respectively. Vectors and matrices are denoted by lower-case and upper-case letters in bold font, respectively. Impulse response in time-domain is represented by lower-case letter with an index *n*. Filter response in *z*-domain is represented by upper-case letter in bold font.

2. Signal models

This section provides parametric data models of multiple RF sources with the wavelength λ impinging on an uniform circular array (UCA) evenly spaced on ring of radius *R*. Suppose that we have *M* antenna elements ($M \geq 3$) and *P* narrow band far-field signals. The signal sources may be uncorrelated, highly correlated or fully correlated (referred as coherent signals).

Let $s_p(t)$ be signals arrived at the center of UCA with bearing angle θ_p, where $p = 0, \ldots, P-1$. The signals received by the *m*-th antenna element can be described as

$$x_m(t) = \sum_{p=0}^{P-1} a_m(\theta_p) s_p(t) + n_m(t), \quad m = \overline{0, M-1} \tag{1}$$

where $n_m(t)$ denotes the noise at the *m*-th antenna element; and

$$a_m(\theta_p) = \exp\left(j \frac{2\pi R}{\lambda} \cos\left(\frac{2\pi m}{M} - \theta_p \right) \right) \tag{2}$$

We denote

$$\mathbf{a}(\theta_p) = \left[a_0(\theta_p)\ a_1(\theta_p)\ \ldots\ a_{M-1}(\theta_p) \right]^T \tag{3}$$

where $\mathbf{a}(\theta_p)$ represents the steering vector of the array toward direction θ_p.

In matrix notation, (1) becomes

$$\mathbf{x}(t) = \mathbf{A}(\Theta)\mathbf{s}(t) + \mathbf{n}(t) \tag{4}$$

where $\mathbf{x}(t)$, $\mathbf{s}(t)$ and $\mathbf{n}(t)$ are vectors,

$$\mathbf{x}(t) = \left[x_0(t)\ x_1(t)\ \ldots\ x_{M-1}(t) \right]^T \in \mathbb{C}^{M \times 1} \tag{5}$$

$$\mathbf{s}(t) = \left[s_0(t)\ s_1(t)\ \ldots\ s_{P-1}(t) \right]^T \in \mathbb{C}^{P \times 1} \tag{6}$$

$$\mathbf{n}(t) = \left[n_0(t)\ n_1(t)\ \ldots\ n_{M-1}(t) \right]^T \in \mathbb{C}^{M \times 1} \tag{7}$$

and $\mathbf{A}(\Theta)$ is the *M* x *P* matrix of the steering vectors,

$$\mathbf{A}(\Theta) = \left[\mathbf{a}(\theta_0)\ \mathbf{a}(\theta_1)\ \ldots\ \mathbf{a}(\theta_{P-1}) \right] \in \mathbb{C}^{M \times P} \tag{8}$$

In the case, where only one signal $s(t)$ arrived at the center of UCA with directions of arrival θ, the array response model is:

$$\mathbf{x}(t) = \mathbf{a}(\theta) s(t) + \mathbf{n}(t) \tag{9}$$

In practice, the received signals are likely to contain energy of other signal

sources at frequencies around the frequency band of interest and noises, for example, interference from other users of the radio channel. If filtering techniques can attenuate energy of unwanted signal sources and noise as far as possible, then these unwanted signal sources can be treated as noise. So that, the signal can be successfully received. This is part of the DDC's job.

3. Proposed hardware architecture description

This section provides description of the proposed hardware architecture. The high-level block diagram is shown in Fig. 1. It consists of four main blocks: memory, frequency tracker, DDCs processing chain and correlation interferometer.

The memory block stores the samples of input signals from the ADCs (analog-to-digital converters) to create a delay memory function. Delayed data from memory block feeds the inputs of DDCs. The digital delay can be set to match the time it takes for the FFT calculation, the FFT energy detection and frequency detection algorithm for the tuning frequency decision. Next, we will detail the remaining blocks.

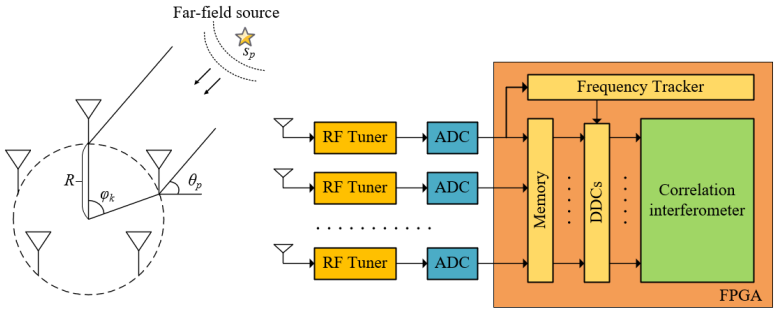


Fig. 1. High-level block diagram of the proposed hardware architecture of the DOA estimator

3.1. Frequency tracker block

Frequency tracker has the ability to detect the presence of unknown frequencies, lock onto them and track them. This block includes an FFT IP (intellectual property) core and weighted frequency tracking unit (see Fig. 2).

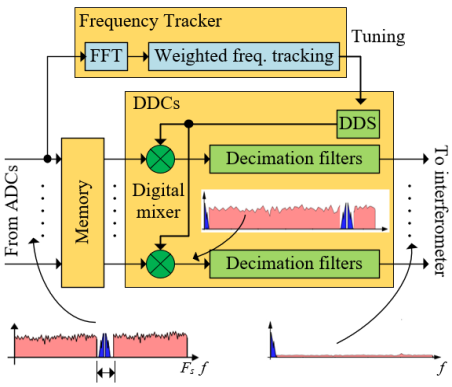


Fig. 2. Hardware architecture of the frequency tracker and the DDCs blocks

Samples from M ADC are delivered into memory which acts as a digital delay memory while samples from one ADC are also delivered into an FFT IP core. FFT core converts a sequence of N time domain samples $x(n)$ to a representation sampled in the frequency domain at N discrete frequencies or "bins" $X(k)$ as follows:

$$X\left(k\right)=\sum_{n=0}^{N-1}x(n)e^{-j2\pi kn/N},\quad k=\overline{0,N-1} \tag{10}$$

where N is the FFT transform size. The parameter N is usually chosen to be a power of two, i.e. $N = 2^n$, where n is an integer.

We assume that the sampling frequency is F_s, the spacing between the frequency components is

$$\Delta f=\frac{F_s}{N}=\frac{1}{NT_s} \tag{11}$$

The larger the value of N, the more frequency bins available and therefore the more accurate the spectrum produced. However, more the delay time for the FFT calculation, for the FFT energy detection and tuning frequency decision. It requires a more size of memory and cannot guarantee the real-time signal processing requirements. To solve this problem, the weighted frequency tracking algorithm applied for a small FFT size is proposed.

The weighted frequency tracking unit detects the strength of signals at each analysis frequency, digests this frequency list according to peak strength and decides which signals to track.

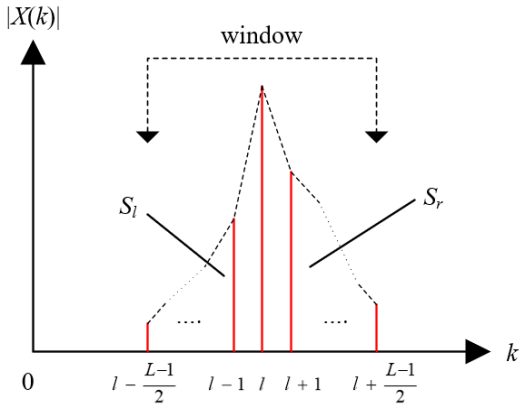


Fig. 3. The window and areas presentation

The strongest signal frequencies can be used to tune the DDCs. However, the proposed weighted frequency tracking algorithm allows detect the more accurate tuning frequencies as follows. The weighted frequency tracking unit locates windows of frequency samples so that the center of the windows is tuned to the strongest signal

frequencies. We assume that the size of window is L, L is an odd integer, the position of the strongest signal frequency bin is l, then tuning frequency f_{DDS} of DDCs can be represented as:

$$l_{tune} = l + \frac{S_r - S_l}{|X(l)|} \tag{12}$$

$$f_{DDS} = l_{tune}\Delta f \tag{13}$$

where S_r is the area of trapezoids formed from the $X(k)$ ($k = l, l+1, ..., l+\frac{L-1}{2}$) and the k-axis, S_l is the area of trapezoids formed from the $X(k)$ ($k = l, l-1, ..., l-\frac{L-1}{2}$) and the k-axis (see Fig. 3).

3.2. DDCs processing chain

The DDC function is to translate a passband signal comprising one or more radio or intermediate frequency (RF or IF) carriers to one or more baseband channels, filter and down the input RF/IF sample rate to the baseband processing sample rate of the system. The DDC can also perform frequency translation to shift each frequency band of interest to baseband. Frequency band selection filtering is normally incorporated into the filtering functions of DDC modules, and the sample rate conversion is normally performed most efficiently over multiple stages, with appropriate low-pass filtering for anti-aliasing or image rejection. The general architecture of a DDC therefore consists of multiple stages of filters and mixers, with the mixers being constructed variously from direct digital synthesizers (DDS) [13] and multipliers. This generalized architecture is illustrated in Fig. 2.

The digital mixers and DDS translate the digital RF/IF samples down to baseband. At the output of the mixers, the high frequency wide-band signals from the ADC input have been translated down to baseband or DC and up to higher frequency band with a frequency shift equal to the frequency of DDS (see Fig. 2).

The decimation filters limit the signal bandwidth and act as a decimating lowpass filters to remove adjacent channels, minimize aliasing, maximize the received signal-to-noise ratio (SNR) and reduce the sample rate. The bandwidth of the signal of interest is significantly less than the sampled bandwidth. This means that large sample rate changes (in the hundreds or even thousands) must be undertaken to efficiently process the signal.

When the desired sample rate change is 32 or more, it is advisable to consider the use of CIC (cascaded integrator-comb) filters [14]. CIC filters are well-suited to large

sample rate changes, as they can be implemented efficiently in FPGAs (see Fig. 4). The CIC filter is characterized by the impulse response in time-domain and *z*-domain as

$$h_{CIC}(n)=\begin{cases}1, & 0\le n\le R-1\\ 0, & \text{otherwise}\end{cases} \tag{14}$$

$$\boldsymbol{H}(z)=\left(\frac{1-z^{-R}}{1-z^{-1}}\right)^{N}=\boldsymbol{H}_1(z)\boldsymbol{H}_2(z) \tag{15}$$

where

$$\boldsymbol{H}_1(z)=\left(\frac{1}{1-z^{-1}}\right)^{N} \tag{16}$$

$$\boldsymbol{H}_2(z)=\left(1-z^{-R}\right)^{N} \tag{17}$$

R is decimation ratio and *N* is number of stages in filter.

The CIC filters are constructed from integrator and comb filter stages. Decimation CIC filters require a cascade of a number of integrator units $\boldsymbol{H}_1(z)$, followed by a down-sampling stage and finally a cascade of the comb filter units $\boldsymbol{H}_2(z)$. CIC filters use only delays and summation units and do not require multiplication operations.

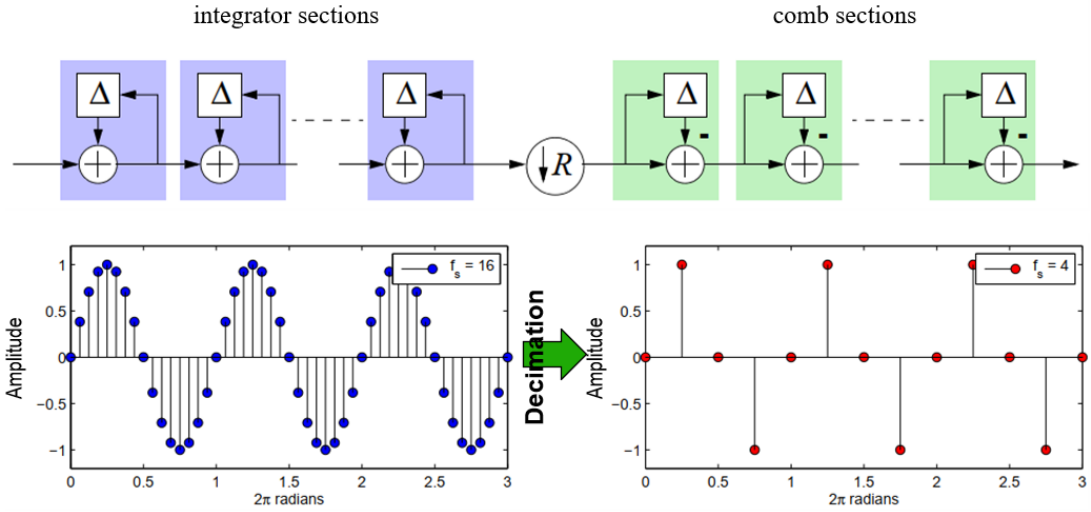


Fig. 4. Structure of the decimation CIC filter and its decimating processing

The frequency response of a CIC filter exhibits a sinc-like function, as illustrated in Fig. 5. The frequency response of CIC filters is affected by several parameters: the rate change, *R*, and the number of stages, *N*. The droop characteristic of the CIC may significantly distort the passband and require correction in some way. A candidate solution to this problem is to insert a compensation filter, designed to provide the appropriate corrective lift in the passband region.

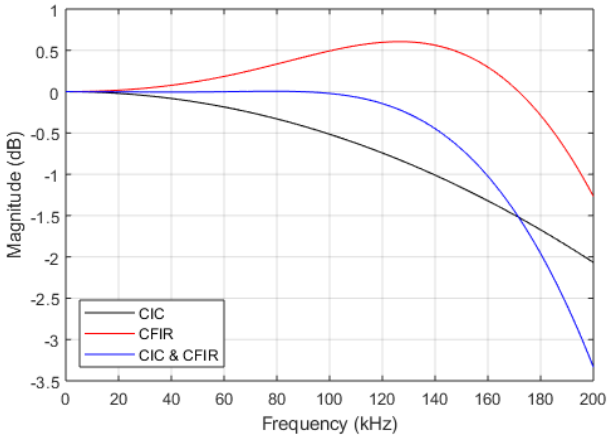


Fig. 5. Amplitude-frequency characteristic of the CIC, CFIR filters and their cascade

Finite Impulse Response (FIR) filter with an inverse-sinc frequency response is often used as a compensation filter (CFIR). The impulse response of a FIR filter of order N as defined is nonzero over a finite duration and represented in time-domain and z-domain as follows [15]:

$$h_{fir}(n) = \sum_{i=0}^{N} w_i \delta[n-i] \begin{cases} w_n, & 0 \le n \le N \\ 0, & \text{otherwise} \end{cases} \tag{18}$$

$$\boldsymbol{H}_{fir}(z) = \sum_{i=0}^{N} w_i z^{-i} \tag{19}$$

where $\delta(n)$ is a Kronecker delta function; b_i, $i = 0, 1,..., N$, are coefficients of filter.

Often the CFIR incorporates a decimation step of two, which may reduce the number of stages (and therefore resources) required in the CIC filter. As we can see that in the filter response of the cascade of the two filters (Fig. 5), which is between the CIC response and the compensating FIR response, the passband droop has been eliminated.

Another option is that programmable FIR filter (PFIR) is used to achieve a high decimation ratio, aliasing attenuation and application-specific filtering. The PFIR block filters the signal to meet the requirements of specific baseband spectral mask. The PFIR filter can be designed by using a low-pass FIR filter (18), (19) [15]. This filter can also perform a rate change by 2, thus reducing the requirements for the CIC filter.

3.3. Correlation interferometer

Due to its ease of implementation and low computational complexity, the correlative interferometer principle has gained popularity in most of modern direction finding products. In principle, the correlative interferometer direction finding algorithm consists of two steps. The novel contributions in the interferometer lie in both steps.

• *Phase difference estimation*: Estimate the phase differences between input signals incoming from pairs of antenna elements.

• *Phase difference evaluation*: Calculate the direction of arrival of RF signals by correlating the estimated phase difference.

Because the signals at the outputs of DDCs, $u_i(n)$, i = 0, 1, …, M – 1, have the frequency and phase which are translated with a frequency and phase shift equal to the frequency and initial phase of DDS, therefore, the phase differences between input signals incoming from pairs of antenna elements equal to that of the respective output signals of DDCs, and

$$\mathbf{u}(n) = \mathbf{a}(\theta)\tilde{s}(n) + \tilde{\mathbf{n}}(n) \tag{20}$$

$$\mathbf{u}(n) = \left[u_0(n)\ u_1(n)\ \ldots\ u_{M-1}(n)\right]^T \in \mathbb{C}^{M\times 1} \tag{21}$$

$$\tilde{\mathbf{n}}(n) = \left[\tilde{n}_0(n)\ \tilde{n}_1(n)\ \ldots\ \tilde{n}_{M-1}(n)\right]^T \in \mathbb{C}^{M\times 1} \tag{22}$$

where $\tilde{\mathbf{n}}(n)$ is the noise vector filtered at the outputs of DDCs; $\tilde{s}(n)$ presents a modified version of the signal $s(n)$ shifted frequency and phase equal to the frequency and initial phase of DDS; $s(n)$ is the discretized signal of $s(t)$ in (9).

We assume that noises $\tilde{n}_i(n)$ are uncorrelated and they are uncorrelated with the sourced signals $u_i(n)$, i = 0, 1, …, M – 1. Let us consider the cross-correlation between two consecutive signals at the outputs of DDCs.

$$\begin{aligned} y_i(n) &= u_i(n)u^*_{(i+1)\bmod M}(n) \\ &= \tilde{s}(n)\tilde{s}^*(n)a_i(\theta)a^*_{(i+1)\bmod M}(\theta) + \tilde{n}_i(n)\tilde{n}^*_{(i+1)\bmod M}(n) \end{aligned} \tag{23}$$

Because the power of filtered noises at the outputs of DDCs is very small, (23) can be written as:

$$y_i(n) \approx \tilde{s}_i(n)\tilde{s}(n)a_i(\theta)a^*_{(i+1)\bmod M}(\theta) \tag{24}$$

From (2) we have

$$a_i(\theta)a^*_{(i+1)\bmod M}(\theta) = \exp\left(j\frac{4\pi R}{\lambda}\sin\left(\frac{\pi}{M}\right)\sin\left(\frac{2\pi i}{M} - \frac{\pi}{M} - \theta\right)\right) \tag{25}$$

The cross-correlation signals $y_i(n)$ are obtained by using the complex multipliers in FPGA. The phase of signals $y_i(n)$ can be estimated based on CORDIC Artan (COordinate Rotation DIgital Computer) algorithm [16].

$$\phi_i = \frac{4\pi R}{\lambda}\sin\left(\frac{\pi}{M}\right)\sin\left(\frac{2\pi i}{M} - \frac{\pi}{M} - \theta\right) \tag{26}$$

DOA values θ can be obtained by using trigonometric operators and CORDIC Artan function. In this paper, DOA estimation algorithm is given for M = {3, 4, 5}. For other values of M, DOA estimation algorithm can be obtained similarly.

For M = 3

$$\theta = \arctan\frac{\sqrt{3}\phi_2}{\phi_1 - \phi_0} \tag{27}$$

For M = 4

$$\theta = -\arctan\frac{\phi_0 + \phi_1}{\phi_3 - \phi_2} \tag{28}$$

For M = 5

$$\theta = \frac{3\pi}{5} - \arctan\frac{2\left[\sin\frac{4\pi}{5} + \sin\frac{2\pi}{5}\right]\phi_2}{(\phi_4 + \phi_3) - (\phi_0 + \phi_1)} \tag{29}$$

4. Experimental results

In this paper, the performance of the proposed hardware scheme of DOA estimation receiver is evaluated. System Generator for DSP tool is selected in the design, because it is a system-level modeling tool from Xilinx that enables the use of the MathWorks model-based Simulink design environment for FPGA design. System Generator for DSP tool is a flexible high-level system modeling environment. In a System Generator design, signals are not just bits. They can be signed and unsigned fixed-point numbers, and changes to the design automatically translate into appropriate changes in signal types. That is generally preferred for DSP applications which often require fixed-point arithmetic operations. Simulations in System Generator are considerably faster than those from the traditional HDL simulators, and results are easier to analyze.

Assume that the RF/IF input of DOA estimation system includes noises and signal carriers of 20.05, 43.92 and 70.05 MHz. The signal with frequency carrier of 43.92 MHz is the strongest (Fig. 6) and arrives at the center of UCA with directions of arrival of π/4. The sampling frequency of ADC is 200 MHz. The number of antenna elements in UCA is 5.

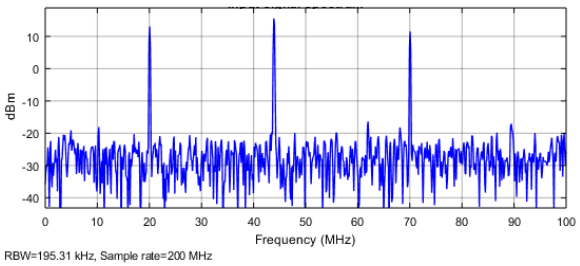
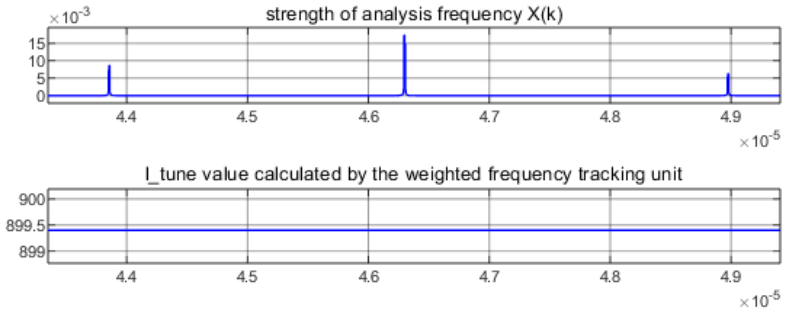
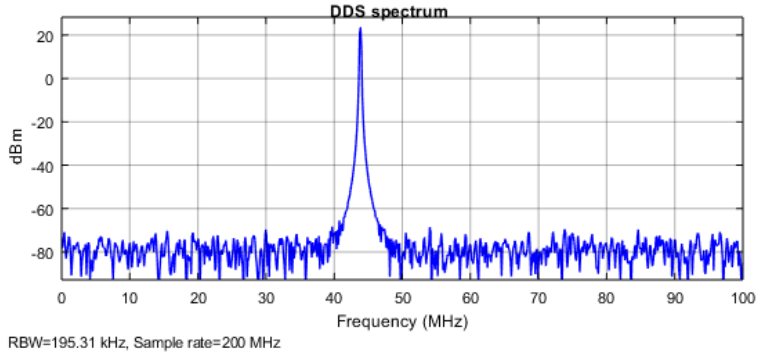


Fig. 6. Spectrum of incoming signals and noises

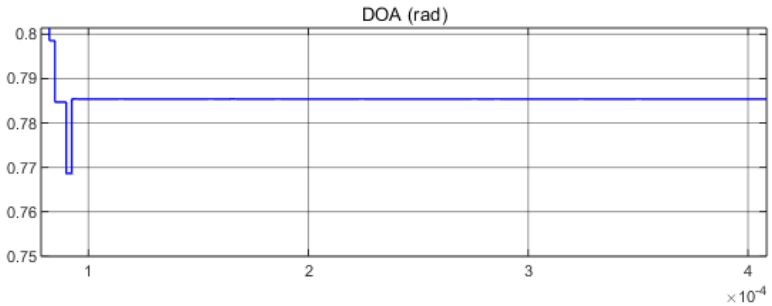
Received results from the System Generator for DSP tool in Fig. 7 show that 4096-point FFT gives three peaks, the weighted frequency tracking unit locks onto the analysis frequency index of 899 and calculates the l_{tune} value (about 899.4). Hence, value of f_{dds} = 200e6/4096l_{tune} ≈ 43.916 MHz. If the weighted frequency tracking unit is not used, l_{tune} will lock onto value of 899. In this case, f_{dds} = 899×200e6/4096 = 43.896 MHz. Therefore, the frequency of DDS is more accuracy calculated, when the weighted frequency tracking unit is used. Also, from Fig. 7, DOA estimation value is about 0.7854 ≈ π/4 radian.



(a)



(b)



(c)

Fig. 7. Received results on System Generator for DSP tool: (a) Strength of the frequency components on the FFT output; (b) Signal generated by the DDS; (c) DOA estimation result.

The proposed hardware architecture of the DOA estimation receiver described in this paper has been implemented and tested on Xilinx FPGA chip using the ML507 board and ADC board (see Fig. 8). The ADC board includes six 10-bit ADCs AD9211-250 which operates up to 250 MSPS conversion rate. To indicate experimental results, the ML507 board is connected to a computer and VGA/LCD display. The DOA estimation values are transmitted to the computer via a simple serial interface RS-232. These DOA estimation values are also presented on VGA/LCD screen. The experimental signal is generated in a frequency hopping transmitter located at different directions. The transmitting radio signals of this transmitter change in available frequency band of 5-100 MHz. The clock frequency of FPGA F_{clk} and conversion rate of ADCs F_s is 234 MHz. This clock frequency is selected to work with standard monitors at the 1920x1440@60Hz VGA mode. The number of ADCs connected to FPGA is 4 (therefore, the number of antenna elements is M = 4) and only six MSB bits of these ADCs are used. This is because the number of FPGA I/Os (input/output pins) on the expansion header of ML507 board is 32.

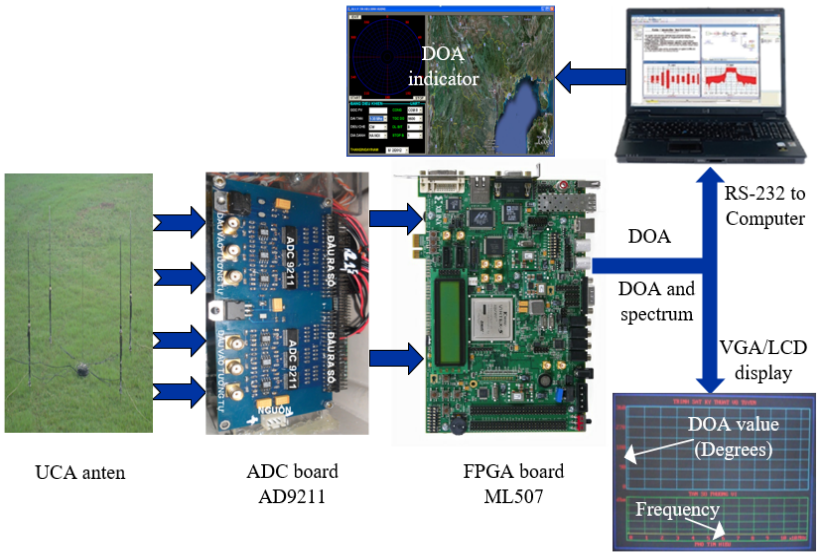
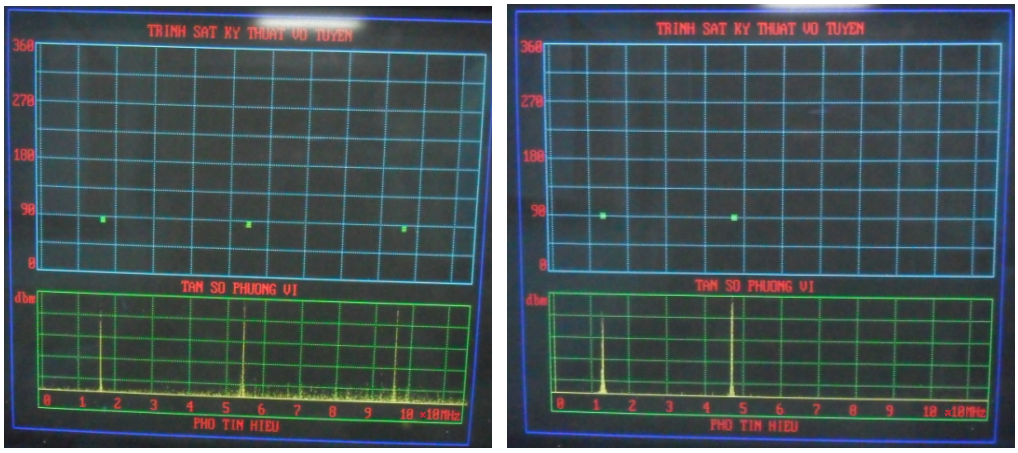


Fig. 8. Experimental setup of the proposed DOA estimation receiver

The 4096-point FFT is used in experiments. From equation (11) the spacing between the frequency components $X(k)$ is $\Delta f = F_s/N_{FFT}$ = 234/4096 ≈ 57.129 kHz. Maximum carrier frequency of the experimental transmitting signal is f_{max} = 100 MHz. Therefore, the maximum frequency component $X(k)$ on the FFT output approximated to f_{max} has index $k_{max} = f_{max}/\Delta f$ = 1750. 1751 amplitude values of $X(k)$, k = 0, 1,..., k_{max}, are displayed on the center of the screen corresponding to 1751 of 1920 pixels (see Fig. 9).



(a) *(b)*

Fig. 9. Display results on VGA/LCD monitor: (a) when three signal frequencies are observed on the screen; (b) when two signal frequencies are observed on the screen.

From Fig. 9 can see that the signal frequency is hopped. One observation can see 2-3 carriers. The DOA values are estimated and displayed at locations corresponding to each carrier frequency. They are similar with angle values about 90 degrees, because the position of the transmitter is unchanged. These DOA values are also transmitted to PC and presented on the indicator (green line in Fig. 10). Fig. 10 shows that the indication lines (green line) are located at the angle of 90 degrees.

Experimental results at the angle of 45 degrees are shown in Fig. 11. When the transmitter changes carriers with a small frequency value, the proposed DOA estimation receiver has ability to track them and estimates truly DOA. This can be seen in Fig. 11a. Two of three carriers have frequency values which vary a small amount. Their estimated DOAs are similar and have value of 45 degrees. The indication lines on computer are indicated at the corresponding angle (45 degrees).

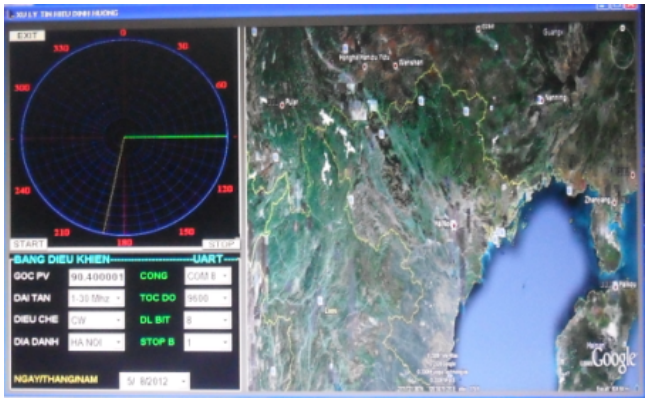
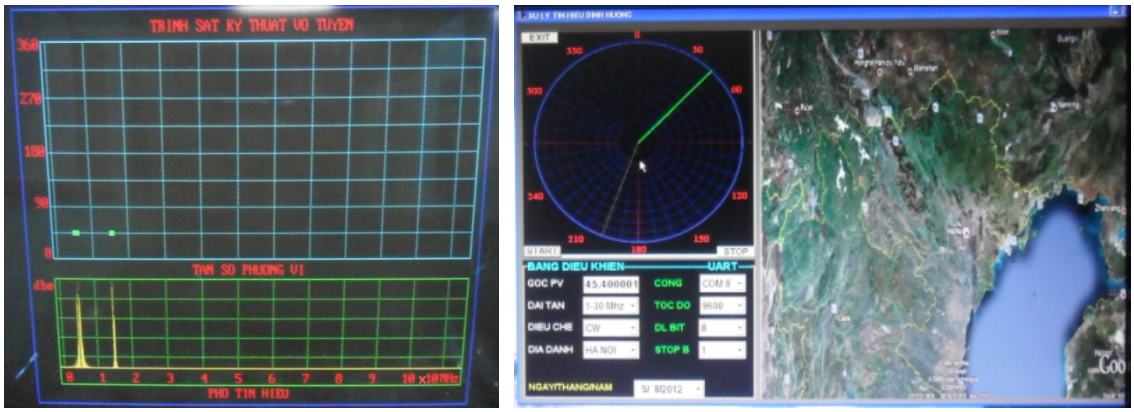


Fig. 10. DOA indicator at 90 degrees on computer.



(a) *(b)*

Fig. 11. Experimental results at the angle of 45 degrees:
(a) on VGA/LCD monitor; (b) on PC indicator.

In the expriments, at the each position of the transmitter, the transmitting radio signals are changed with the frequency hop step of 100 kHz. The experimental parameters and results of these trials are shown in Tab. 1. The proposed receiver estimates independently the signal frequency and its DOA, so the received estimation results of the frequency and DOA are independent of each other. The mean values of DOA estimates were calculated on 10 hopped frequencies. While the mean values of frequency estimates were calculated on 10 positions of the transmitter. The FPGA resource utilisation of the proposed hardware architecture is summarised in Tab. 2.

Tab. 1. The experimental parameters and measurement results

Parameters	**Values**									
Signal frequency (kHz)	5200	12500	14900	16500	47600	54000	65000	72300	80600	97100
Estimated frequency (kHz)	5196	12505	14904	16503	47595	53907	65008	72301	80608	97102
Signal DOA (degrees)	0	30	45	60	90	120	150	180	240	270
Estimated DOA (degrees)	0.1	30.3	45.1	59.2	89.5	119.7	150.2	179.6	239.3	269.6

Tab. 2. FPGA resource utilisation of the proposed hardware architecture

Device resources	**Available**	**Used**	**Utilisation**
Slice look-up-tables (LUTs)	44,800	9,874	22%
Slice registers	44,800	11,150	24%
Block RAM tile	148	20	13%
DSP48E	128	116	91%
Maximum frequency (MHz)	318.288		
Output latency (clock cycles)	4208		

From Tab. 1 can see that the estimated DOA results are close to the actual angles (the DOA estimation accuracy is smaller than 1 degree). The frequency estimation accuracy is below 10 kHz for the transmitting frequency band of 5-100 MHz. The frequency and DOA estimation accuracy is suitable for electronic attack systems, in which noise jammers place a signal into the receiver to interfere with the reception or processing of the desired signal [17].

The processing delay is 4208 clock cycles (approximates to the FFT size, see Tab. 2), i.e. it is equal to $4208*T_{clk} \approx 16$ μs. While existing fast frequency hopping systems can achieve up to 5000 hops, but not faster, because a synchronization is required between the transmitter node and the receiver node. The existing time of each frequency of the transmitting signal is 0.2 ms. Therefore, the processing delay of the proposed hardware architecture can guarantee that the noise jammer attacks the receiver within the existing duration of the signal.

Compared to the hardware architectures proposed in [4, 7], the hardware architecture in this paper requires a very small FPGA resource utilisation. This is because, the proposed architecture uses a small number of antennas (hence, it uses a few number of DDCs blocks in compared to [4]) and does not use the matrix operations. Moreover, the frequency tracker used in the proposed architecture tunes the center frequency of the DDCs that makes it suitable to estimate the DOA of frequency hopping communication systems. This feature is not obtained in [4, 7].

5. Conclusions

In this paper, the author has proposed the DOA estimation receiver including frequency tracker, DDCs and correlation interferometer, and implemented it on FPGA. The proposed hardware architecture has a low complexity and more suitable for DOA estimation of frequency hopping communication systems. The simulation results of the proposed signal processing hardware architecture on the System Generator for DSP Tool and its FPGA implementation show that the proposed receiver has the ability to lock, track and estimate the frequency hopping signals.

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THỰC THI ƯỚC LƯỢNG GÓC HƯỚNG HIỆU SUẤT CAO SỬ DỤNG MẢNG ĂNG TEN TRÒN ĐỒNG NHẤT TRÊN FPGA

Tóm tắt: *Trong bài báo này, tác giả trình bày kiến trúc phần cứng xử lý tín hiệu để khóa tần số tín hiệu quan tâm có ở đầu vào, bám chúng nếu tần số thay đổi và ước lượng góc hướng đến (DOA) của tín hiệu quan tâm bằng cách sử dụng mảng ăng ten tròn đồng nhất. Kiến trúc phần cứng đề xuất được mô tả chi tiết, được thực thi và kiểm chứng bằng các thử nghiệm thực tế trên chip FPGA. Các kết quả thử nghiệm cho thấy rằng độ chính xác ước lượng DOA nhỏ hơn 1 độ. Độ chính xác ước lượng DOA này phù hợp với các hệ thống tấn công điện tử.*

Từ khóa: Góc hướng đến; bộ đảo tần xuống số; bộ bám tần số; bộ so pha tương quan; mảng ăng ten tròn đồng nhất.

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