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# HYBRID MULTILEVEL INVERTER COMBINING 3-LEG INVERTERS AND H-BRIDGE MODULES FOR SOLAR PHOTOVOLTAIC APPLICATIONS

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**ABSTRACT**

The rapid deployment of renewable energy technologies has significantly accelerated the adoption of solar photovoltaic systems in modern power networks. In this study, a hybrid multilevel inverter (HMI) architecture, consisting of a three-leg voltage source inverter combined with H-bridge modules and an output LC filter, is proposed for standalone photovoltaic applications. The system is capable of supplying balanced and unbalanced nonlinear AC loads while maintaining voltage quality. A multi-carrier PWM strategy together with a proportional–integral voltage controller is implemented to regulate the output voltage. The operational performance of the proposed inverter is verified through detailed PSIM-based simulations.

*Keywords:* Hybrid multilevel inverter, standalone PV system, a 3-leg inverter, H-bridge.

## 1. INTRODUCTION

Solar energy is widely regarded as an environmentally friendly and sustainable resource capable of addressing the continuously increasing global electricity demand. In practical applications, solar photovoltaic (PV) technology enables the direct conversion of solar irradiation into usable electrical energy. This form of energy has been deployed across numerous sectors, among which standalone PV systems have attracted considerable attention. Such off-grid configurations integrate PV arrays, energy storage units, and power electronic converters to ensure a stable electricity supply for remote and isolated areas lacking access to the utility grid [1].

In PV systems, the inverter is crucial for maintaining efficient power conversion and system stability. It also ensures that the power output matches the needs of the load, especially when there are variations in solar power generation. To achieve higher performance and quality, multilevel inverters have become increasingly popular in PV systems [2]. Multilevel inverter topologies offer superior output voltage quality by effectively suppressing harmonic components relative to conventional two-level inverters [3]. In this context, the cascaded H-bridge (CHB) inverter is particularly appealing due to its modular architecture, flexible scalability, and its capability to generate near-sinusoidal output voltages using a reduced number of power switches.

The hybrid cascaded H-bridge inverter demonstrates strong operational stability and dependable performance under varying load and operating conditions [4]. This inverter structure synthesizes multilevel output voltages by interconnecting several H-bridge cells supplied from independent DC links, thereby contributing to the mitigation of harmonic distortion and a reduction in switching-related losses [5]. Despite these advantages, the topology requires a relatively large number of power modules and separate DC supplies, which increases system complexity and results in higher implementation costs.

To overcome the aforementioned limitations, this study introduces a hybrid multilevel inverter architecture that integrates a three-leg voltage source inverter with auxiliary H-bridge modules. Compared with the conventional cascaded H-bridge configuration, the proposed structure requires a smaller number of power components and DC supplies, which contributes to reduced system complexity and lower implementation cost. Furthermore, the H-bridge modules can be incorporated incrementally to adapt the inverter to different photovoltaic system capacities and operating demands [6]. By combining the operational characteristics of both three-leg and H-bridge inverters, the proposed topology achieves improved reliability, a reduced component count, and enhanced expandability, thereby offering a practical solution for standalone photovoltaic applications.

This paper evaluates the performance of the proposed hybrid multilevel inverter (HMI) in standalone PV system, focusing on its ability to maintain the desired output voltage with minimal distortion. A classical PI controller integrated with a multi-carrier pulse width modulation (MCPWM) scheme is employed to achieve precise voltage regulation. The system's functionality and effectiveness are validated through comprehensive simulations using PSIM software, highlighting its potential as a cost-effective and reliable solution for solar PV applications.

## 2. SYSTEM MODELING

### 2.1. HMI combines a 3-leg inverter with H-bridge modules

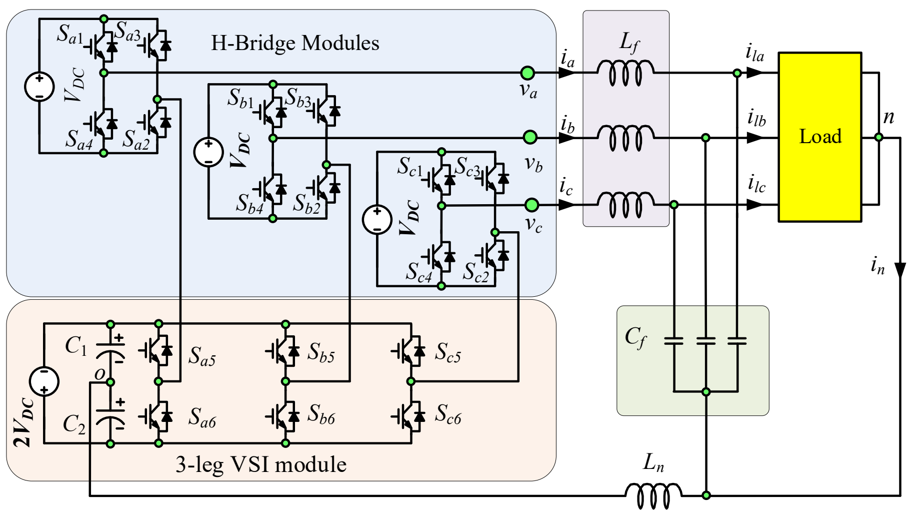



*Figure 1*. Topology of HMI based on 3-leg VSI

The proposed three-phase inverter architecture is formed by integrating two functional parts. A three-phase, three-leg, two-level voltage source inverter (3-leg VSI) serves as the primary conversion stage, while additional H-bridge (HB) modules are connected to each phase, as depicted in Figure 1. The H-bridge units operate with a DC-link voltage of $V_{DC}$, whereas the main inverter is supplied by a DC voltage of $2V_{DC}$. This voltage allocation enables the synthesis of a five-level output waveform [7, 8]. All DC-link voltages are provided by photovoltaic sources. Moreover, the inverter configuration supports the incorporation of additional H-bridge modules to increase the number of output voltage levels without requiring structural modifications to the original system.

The output terminals of the hybrid multilevel inverter are connected to an LC filter before supplying a standalone load. In practical applications, the load may operate under asymmetric conditions arising from unequal phase loading, the integration of single-phase loads, or abnormal operating states in three-phase systems. Such operating scenarios introduce zero-sequence voltage components at the load side. Conventional three-phase, three-wire inverter topologies are not capable of compensating for these zero-sequence effects, which may lead to voltage imbalance. Therefore, a connection to the load neutral point "n" is required to provide a current path for zero-sequence components and to improve voltage balance at the load terminals [9,10].

The neutral point "o" of the HMI is established using two DC capacitors connected in series and placed between the two poles of the main module's DC source. This method is simple to implement and cost-effective. Under the condition that the voltages across capacitors $C_1$ and $C_2$ remain equal, the three-phase output voltages ($v_a, v_b, v_c$) are generated through appropriate switching actions of each phase leg and can be expressed as:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = V_{DC} \times \left( S \times \begin{bmatrix} 1 \\ -1 \\ 2 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \right) \tag{1}$$

S is the switch state matrix:

$$S = \begin{bmatrix} S_{a1} & S_{a3} & S_{a5} \\ S_{b1} & S_{b3} & S_{b5} \\ S_{c1} & S_{c3} & S_{c5} \end{bmatrix} \tag{2}$$

In this notation, $S_{j1}$, $S_{j3}$, and $S_{j5}$ denote the switching variables associated with the H-bridge units and the main inverter for phases $j \in \{a, b, c\}$, respectively, and are defined as follows:

$$S_{ji} = \begin{cases} 1 & \text{when } S_{ji} \text{ on} \\ 0 & \text{when } S_{ji} \text{ off} \end{cases} \quad (i = 1,2,3) \tag{3}$$

From equation (1), the proposed HMI has the following output voltage levels: $-2V_{DC}$, $-V_{DC}$, $0$, $V_{DC}$, $2V_{DC}$.

### 2.2. Mathematical model of the proposed HMI

The mathematical model of the proposed HMI is formulated in the synchronous *d–q–0* reference frame. To properly account for load asymmetry, the zero-sequence components are explicitly included as follows [10]:

$$\dot{i}_{dq} = \frac{1}{L_f} v_{dq} - \frac{1}{L_f} v_{ldq} - j\omega i_{dq} \tag{4}$$

$$\dot{i}_0 = \frac{1}{\left(L_f + 3L_n\right)} v_0 - \frac{1}{\left(L_f + 3L_n\right)} v_{l0} \tag{5}$$

$$\dot{v}_{ldq} = \frac{1}{C_f} i_{dq} - \frac{1}{C_f} i_{ldq} - j\omega v_{ldq} \tag{6}$$

$$\dot{v}_{l0} = \frac{1}{C_f} i_0 - \frac{1}{C_f} i_{l0} \tag{7}$$

In these equations, $L_f$, and $C_f$ correspond to the filter inductance and the filter capacitance, respectively, while $L_n$, denotes the neutral inductance. The variables $v_d$, $v_q$, and $v_0$ describe the inverter output voltages expressed in the *d–q–0* reference frame, whereas $v_{ld}$, $v_{lq}$, and $v_{l0}$ represent the corresponding load voltages. Similarly, $i_d$, $i_q$, and $i_0$ indicate the inverter output currents, and $i_{ld}$, $i_{lq}$, and $i_{l0}$ denote the load currents in the same coordinate system. The parameter ω refers to the angular frequency of the source.

## 3. CONTROL STRATEGY

### 3.1. Multi-carrier PWM implementation

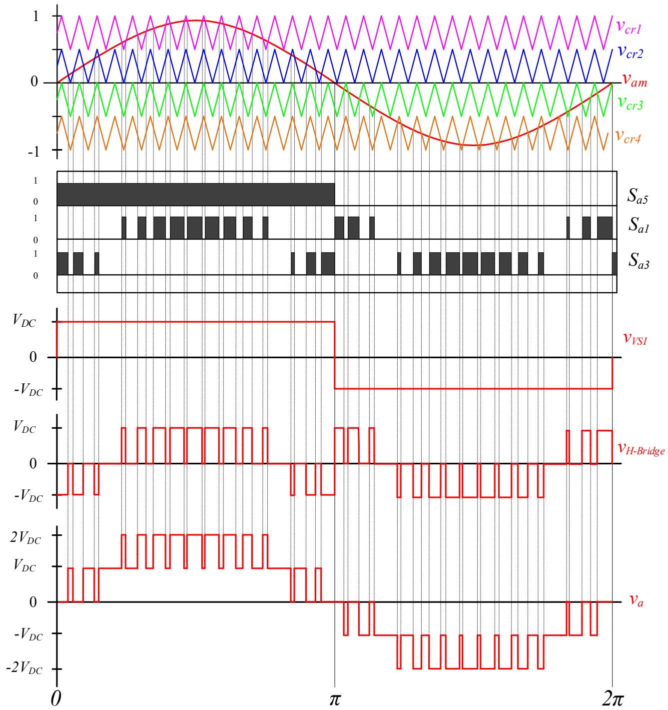



*Figure 2*. Signals for controlling and output waveform of the proposed HMI

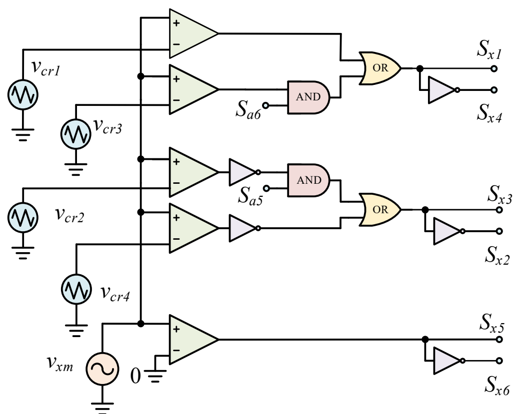



*Figure 3*. PWM generation logic

Figure 2 illustrates the output waveform on phase a of the hybrid multilevel inverter that combines a 3-leg inverter with H-bridge modules, which serves as the reference pattern for generating the control signals for this HMI. Based on MCPWM technique, $n$ - 1 carrier ($v_{cr1}$, $v_{cr2}$, $v_{cr3}$, and $v_{cr4}$). All carrier signals are selected to operate at an identical frequency and amplitude. The sinusoidal modulation signal $v_{am}$ is then evaluated against each carrier waveform to derive the corresponding switching commands.

In the proposed modulation strategy, the switching signals of the main three-leg inverter are generated independently of the carrier comparison process. Specifically, when the reference modulation waveform is positive, the corresponding phase leg of the main inverter is forced to produce a voltage level of $V_{DC}$, whereas a voltage level of -$V_{DC}$ is applied during the negative half-cycle. Consequently, the switching commands of the main module are obtained through a zero-crossing comparison of the modulation signal. In contrast, the H-bridge modules are controlled using a multi-carrier PWM scheme, where sinusoidal reference signals are compared with four phase-synchronized triangular carriers, as illustrated in Figure 3. This modulation arrangement results in low-frequency switching operation for the main VSI, while higher switching frequencies are assigned to the H-bridge modules. Such a switching distribution enables the implementation of low-speed power devices in the three-phase inverter stage, thereby reducing conduction losses in the VSI [11].

### 3.2. Output voltage control

A proportional–integral (PI) controller is employed in this study, as illustrated in Figure 4, and the resulting closed-loop transfer function can be expressed as:

$$\frac{v_l}{v_l^*} = \frac{\sigma s^2 + k_{iv}k_p s + k_{iv}k_i}{L_f C_f s^4 + k_p C_f s^3 + k_{iv}k_p s + k_{iv}k_i} \quad (8)$$

where $\sigma = k_{pv}(k_p + k_i)$ và $\rho = k_i C_f + k_{pv}(k_p + k_i)$

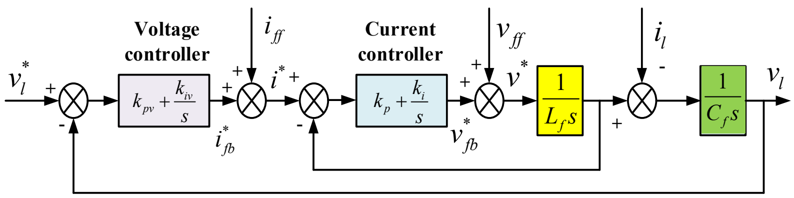



*Figure 4*. Block diagram of the PI controller

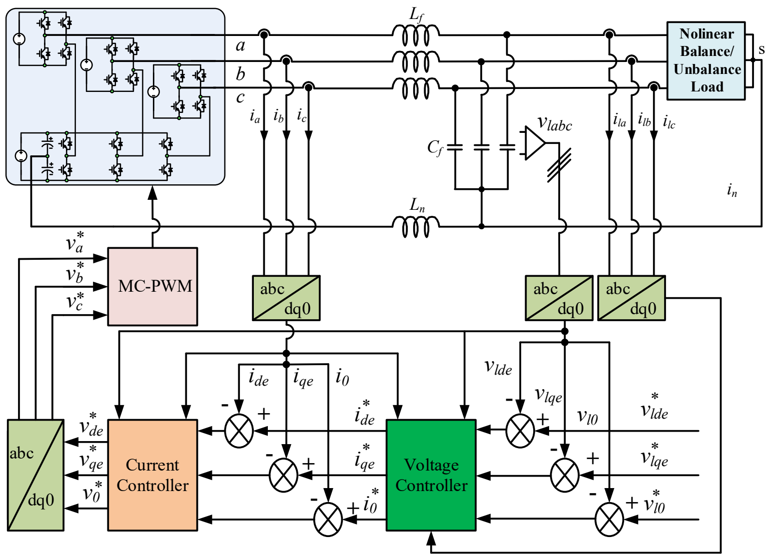


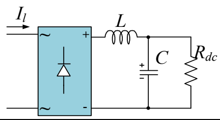
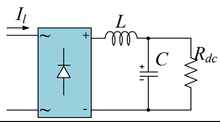

*Figure 5*. Block diagram of the system

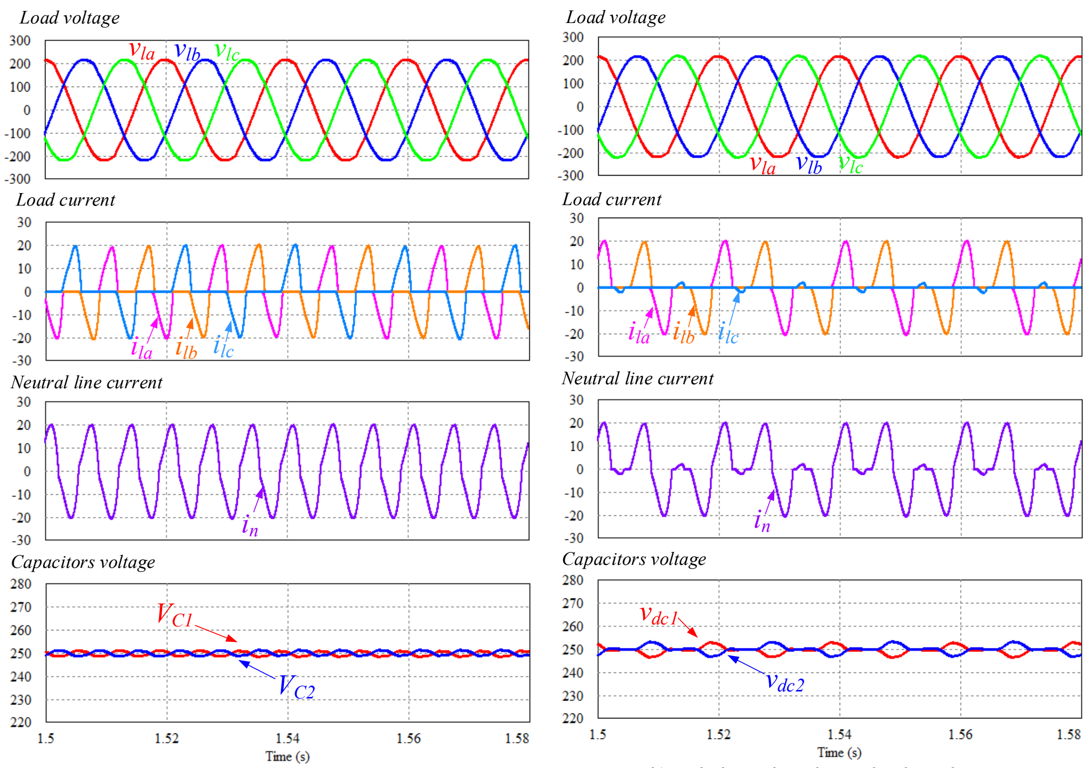
Figure 5 depicts the overall control architecture of the proposed system. The measured voltage and current signals are acquired via sensors and subsequently transformed from the abc reference frame into the *d*-*q*-0 coordinate system for control implementation. The load voltage expressed in *d*-*q*-0 coordinates is compared with its corresponding reference value, and the resulting error is processed by the voltage controller to produce a reference current signal. This reference current is then compared with the inverter output current, and the current controller generates the reference voltage required to govern the IGBT switching through the multi-carrier PWM scheme.

## 4. SIMULATION RESULTS

The performance of the proposed approach is evaluated through PSIM-based simulations under nonlinear and unbalanced load conditions. In the simulation setup, the DC-link voltage of each H-bridge module is specified as 200 V, whereas the main inverter module is supplied with a DC voltage of 400 V. The detailed system configuration and controller settings are summarized in Table 1.

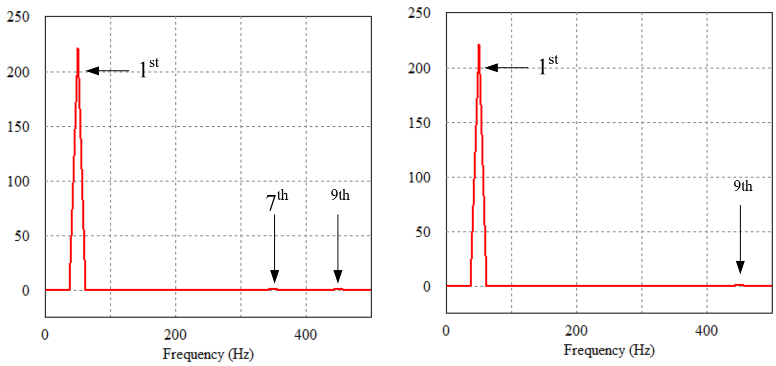
*Table 1*. Simulation parameters

| | ***Parameters*** | ***Value*** |
|---|---|---|
| Output voltage | Amplitude | 220 (V) |
| | Frequency | 50 (Hz) |
| Balance load | Rectifier   | $L$ = 1 (mH), $C$ = 4.7 (mF) $R_{dca} = R_{dcb} = R_{dcc}$ = 50 (Ω) |
| Unbalance load | Rectifier   | $L$ = 1 (mH), $C$ = 4.7 (mF) $R_{dcc}$ = *1 (k Ω)* $R_{dcb} = R_{dca}$ = *50 (Ω)* |
| DC-link | DC source for H-Bridge modules | 200 (V) |
| | DC source for the main module | 400 (V) |
| | $C_{dc1} = C_{dc2} = 2C_{dc}$ | 4.7 (mF) |
| Filter | $L_f$ | 1 (mH) |
| | $C_f$ | 100 (µF) |
| Switching frequency | $f_s$ | 10 kHz |
| PI Controller | Voltage controller | $k_{pv}$ = 12.6, $k_{iv}$ = 9820 |
| | Current controller | $k_p$ = 0.61, $k_i$ = 736 |




*a) Balanced nonlinear load condition* *b) Unbalanced nonlinear load condition*

*Figure 6*. Simulation results of the system




*a) Balance nonlinear load* *b) Unbalance nonlinear load*

*Figure 7*. Fast Fourier transform analysis for phase a load voltage

Figs. 6(a) and 6(b) illustrate the simulation outcomes obtained under balanced and unbalanced nonlinear loading conditions, in which the phase-C load is disconnected. The waveforms presented include the three-phase line-to-neutral output voltages, the corresponding load currents, and the current flowing through the neutral conductor. The results indicate that the nonlinear characteristics of the load introduce current distortion, which leads to the presence of a nonzero neutral current.

In the case of a balanced nonlinear load, the voltage across the load is controlled to follow a sinusoidal waveform, with the total harmonic distortion (THD) for phases a, b, and c being 1.28%, 1.22%, and 1.26%, respectively. Under unbalanced nonlinear load conditions, the load voltage also maintains a sinusoidal waveform, with THD values of 1.14%, 1.32%, and 0.22% for phases a, b, and c, respectively. Figs. 7(a) and 7(b) present the FFT analysis of the phase-a load voltage under balanced and unbalanced nonlinear load conditions, respectively. The FFT results show negligible higher-order harmonic components, which confirms the effectiveness of the proposed control method.

## 5. CONCLUSION

This study has investigated the operational performance of a hybrid multilevel inverter applied to standalone photovoltaic systems, with particular emphasis on output voltage quality. By combining a proportional–integral control strategy with a multi-carrier PWM technique, stable voltage regulation with low distortion is achieved. Simulation results obtained using PSIM demonstrate that the proposed inverter configuration operates effectively under the considered conditions, indicating that the presented approach offers a practical and economical solution for standalone solar PV applications.

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## TÓM TẮT

## ỨNG DỤNG BỘ NGHỊCH LƯU ĐA BẬC LAI DỰA VÀO BỘ NGHỊCH LƯU BA CHÂN VÀ MÔ ĐUN CẦU H VÀO NĂNG LƯỢNG MẶT TRỜI

Nguyễn Ngọc Minh Đoàn[1*], Võ Chí Đại[2], Huỳnh Anh Nhật[2], Trương Quang Huy[3], Trần Thanh Quang[3], Bùi Anh Triều[3], Tạ Quang Vinh[3], Trần Nguyên Dung[4]

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Trong những năm gần đây, các nguồn năng lượng tái tạo đã liên tục tăng cường tích hợp vào các hệ thống điện, đặc biệt là năng lượng mặt trời. Các hệ thống quang điện mặt trời đã trở thành nguồn tài nguyên phổ biến nhất do tiềm năng to lớn của chúng. Trong bài báo này, một bộ nghịch lưu đa bậc lai bao gồm một bộ nghịch lưu 3 chân và các mô đun cầu H, cùng với một bộ lọc LC ở đầu ra đã được đề xuất cho một hệ thống quang điện độc lập, để cấp điện cho tải xoay chiều phi tuyến cân bằng hoặc không cân bằng. Kỹ thuật điều chế độ rộng xung đa sóng mang (PWM) cùng với sử dụng bộ điều khiển tích phân - tỷ lệ cho điều khiển điện áp được sử dụng để duy trì điện áp đầu ra mong muốn. Hoạt động của bộ nghịch đa bậc đề xuất trong hệ thống này được đánh giá và xác thực bằng phần mềm mô phỏng PSIM.

*Từ khóa:* Bộ nghịch lưu đa bậc lai, hệ thống pin quang điện độc lập, bộ nghịch lưu nguồn điện áp 3 chân, mô đun cầu H.