NONLINEAR CONTROL OF THREE-PHASE FOUR-WIRE DYNAMIC VOLTAGE RESTORER UNDER GRID VOLTAGE SAG CONDITIONS

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ABSTRACT

In this paper, a nonlinear control scheme based on backstepping theory for dynamic voltage restorer (DVR) is proposed to mitigate the voltage disturbances for loads under grid voltage sags. A nonlinear model of system with pulse-width modulation (PWM) voltage-source inverter (VSI) including the output inductor-capacitor (LC) filters in the dq0 synchronous reference frames is derived. The controllers of three-phase line-to-neutral load voltages in dq0 components are designed by nonlinear control theory. With the proposed scheme, the load voltage is regulated to reach the rated value and its waveform becomes almost sinusoidal, in comparison with the proportional-integral (PI) controller under grid voltage sags. Simulations are implemented to verify the validity of the proposed method.

Keywords: Dynamic voltage restorer, nonlinear load, backstepping theory, voltage sags, unbalanced load.

1. INTRODUCTION

Recently, the issues of the power quality are paid much attention as the penetration of the renewable energy systems into the grid at the connection point increases quickly. The grid voltage disturbances such as voltage sags, swells, harmonics, unbalances, and flickers are considered as critical power quality issues in distribution systems. Also, the application of power electronics devices in industrial processes, these disturbances influence on the industrial loads. Among these disturbances, the voltage sags are a main reason of short-circuit faults [1-4].

Several devices have been employed to improve the quality of the voltage in the distribution networks such as dynamic voltage restorer system, uninterruptable power supply (UPS), unified power quality conditioner (UPQC), static compensator (STATCOM). Among them, a DVR system is considered as the best solution in order to keep the load voltage at its rated value despite the sudden drop of the grid voltage. The DVR system is made up of a voltage-source inverter, output LC filters, and an isolated transformer connected in series between the source and the loads. Conventionally, both primary and secondary coils of the transformer are connected in Y-windings in distribution systems and the turns ratio is given as 1:1 [5-7].

As for control scheme, a cascaded PI (proportional integral) controller which consists of an outer voltage control and inner current control loops has been employed [8]. However, its control dynamic response is not so fast since the bandwidth of voltage control loop is limited [5]. In addition, there are the negative sequence and zero-sequence components in the source voltage during unbalanced sags conditions. For this, the dq components of the source voltage can be

AC (alternating current) signals. Usually, a typical PI controller cannot control the AC signals well. To overcome this problem, a resonant control has been applied to regulate the UPQC, so that the load voltages are much compensated in the cases of the unbalance and distortion of source voltage and load [9]. However, the algorithms with the PI and PR are both based on the linear control theory, where the performance of the DVR control with a nonlinear model between the inverter terminal voltages and the output capacitor voltages will be considerably deteriorated. Another issue is considering the nonlinearity of the UPS or DVR for control [10, 11]. Thus, the nonlinear control gives better performance than the control techniques based on the PI control.

In the paper, a control method based on backstepping technique has been applied to improve the operation of the three-phase four-wire (3P4W) DVR system under grid fault conditions. First, the nonlinear model of the system including LC filter is obtained in the dq0 synchronous reference frame. Then, the controller design depending on the backstepping control is performed, in which the load voltages are kept almost sinusoidal. Simulation results for 3P4W DVR are provided to verify the validity of the proposed control scheme.

2. SYSTEM MODELING

The three-phase split-capacitor inverter in Figure 1 can be represented in synchronous dq0 reference frame. Due to unbalanced load condition, the zero-sequence components are taken into account as [12, 13]

$$\dot{i}_{dq} = \frac{1}{L_f} v_{dq} - \frac{1}{L_f} v_{ldq} - j\omega i_{dq}$$
(1)

$$\dot{i}_0 = \frac{1}{\left(L_f + 3L_n\right)} v_0 - \frac{1}{\left(L_f + 3L_n\right)} v_{I0}$$
⁽²⁾

$$\dot{v}_{ldq} = \frac{1}{C_f} i_{dq} - \frac{1}{C_f} i_{ldq} - j\omega v_{ldq}$$
(3)

$$\dot{v}_{l0} = \frac{1}{C_f} i_0 - \frac{1}{C_f} i_{l0} \tag{4}$$

where L_f is the filter inductance, L_n is the neutral filter inductance, C_f is the filter capacitance, v_{dq} and v_0 are the dq0 axis inverter output voltages, v_{ldq} and v_{l0} are the dq0 axis phase load voltages, i_{dq} and i_0 are the dq0 axis inverter output currents, i_{ldq} and i_{l0} are the dq0 axis load currents, and ω is the grid angle frequency.

From (1) to (3), a state-space modeling of the system is derived as follows:



Figure 1. Circuit configuration of three-phase four-wire DVR.

3. CONTROL OF DYNAMIC VOLTAGE RESTORER

3.1. Voltage references

The in-phase compensation strategy is considered, in which the amplitude of the load voltage is exactly kept the same as before the sag. Also, the phase of the load voltage is similar to that of the source voltage after the sag. As shown in Figure 1, the load voltage ($v_{L,abc}$) is expressed as:

$$\begin{bmatrix} v_{L,a} \\ v_{L,b} \\ v_{L,c} \end{bmatrix} = \begin{bmatrix} e_{s,a} - v_{dvr,a} \\ e_{s,b} - v_{dvr,b} \\ e_{s,c} - v_{dvr,c} \end{bmatrix}$$
(6)

where $e_{s,a}, e_{s,b}, e_{s,c}$ are the source phase voltage and $v_{dvr,a}, v_{dvr,b}, v_{dvr,c}$ are the phase voltage injected by the DVR.

The DVR control is performed in the electrically rotating reference frame, whereas the phase angle of the source voltage is applied for transforming the DVR output voltages and load voltages. To keep the load voltage to be rated value, the voltage references in the synchronous reference frame (dq0) are calculated as:

$$\begin{bmatrix} v_{dvr,d}^{*} \\ v_{dvr,q}^{*} \\ v_{dvr,0}^{*} \end{bmatrix} = \begin{bmatrix} e_{s,d} - v_{L,d}^{*} \\ e_{s,q} - v_{L,q}^{*} \\ e_{s,0} - v_{L,0}^{*} \end{bmatrix}$$
(7)

where $e_{s,dq0}$ is the components of the source voltage in dq0- axis, and $v_{L,dq0}^*$ is the components of the load voltage references in dq0-axis.

The components of the load voltage references in dq0-axis are obtained as

$$\begin{bmatrix} v_{L,d}^{*} \\ v_{L,q}^{*} \\ v_{L,0}^{*} \end{bmatrix} = \begin{bmatrix} 0 \\ 220V \\ 0 \end{bmatrix}$$
(8)

3.2. Backstepping control

From (5), the dynamic model in the dq0 coordinate system can be expressed as [14]:

$$\dot{Z}_{1.cdq0} = G_1 \dot{i}_{dq0} - G_1 Z_{2.1dq0} + H Z_{1.cdq0}$$
⁽⁹⁾

$$\dot{Z}_{2.1dq0} = F_1 u - F_1 Z_{1.c\,dq0} - H Z_{2.1dq0} \tag{10}$$

where $Z_{1.cdq0} = \begin{bmatrix} V_{c.de} & V_{c.qe} & V_{c0} \end{bmatrix}^T$, $Z_{2.1dq0} = \begin{bmatrix} i_{1.de} & i_{1.qe} & i_{1.0} \end{bmatrix}^T$,

$$G_{1} = \begin{bmatrix} \frac{1}{C_{f}} & 0 & 0\\ 0 & \frac{1}{C_{f}} & 0\\ 0 & 0 & \frac{1}{C_{f}} \end{bmatrix}, \ H = \begin{bmatrix} \omega & 0 & 0\\ 0 & -\omega & 0\\ 0 & 0 & \omega \end{bmatrix}, \ F_{1} = \begin{bmatrix} \frac{1}{L_{f}} & 0 & 0\\ 0 & \frac{1}{L_{f}} & 0\\ 0 & 0 & \frac{1}{L_{f}} + 3L_{n} \end{bmatrix}$$

According to a backstepping control strategy, the system states to track the reference commands are required with two stages [14]. The first stage is that the tracking error of the voltage X_1 is minimized. The current X_2 is controlled with the second stage. Also, the Lyapunov-based scheme has been applied to update the law of the unknown bounded disturbances.

For the stage 1, the errors of the inverter output voltage and load current are expressed as

$$E_1 = Z_{1.cdq0} - Z_{1.cdq0}^*$$
(11)

$$Z_2 = Z_{2.1dq0} - Z_{2.1dq0}^*$$
(12)

where $Z_{1.cdq0}^* = \begin{bmatrix} V_{c.de}^* & V_{c.qe}^* & V_{c0}^* \end{bmatrix}^T$ and $Z_{2.1dq0}^* = \begin{bmatrix} i_{1.de}^* & i_{1.qe}^* & i_{1.0}^* \end{bmatrix}^T$

For tracking error, the derivative of (11) is expressed as

$$\dot{E}_{1} = \dot{Z}_{1.cdq0} - \dot{Z}_{1.cdq0}^{*} = G_{1}\dot{i}_{dq0} - G_{1}Z_{2.1dq0} + HZ_{1.cdq0} - \dot{Z}_{1.cdq0}^{*}$$
(13)

The function of $Z_{2.1dq0}$ is designed to be stabilized as

$$Z_{2.1dq0}^{*} = G_{1}^{-1} \Big(G_{1} \dot{i}_{dq0} + H Z_{1.cdq0} - \dot{Z}_{1.cdq0}^{*} \Big)$$
(14)

Considering (13), (14) and the definition of E_2 , we have

$$\dot{E}_1 = -G_1 E_2 \tag{15}$$

For the stage 2, the derivative of E_2 is expressed as

$$\dot{E}_{2} = \dot{Z}_{2.1dq0} - \dot{Z}_{2.1dq0}^{*}$$

$$= F_{1}u - F_{1}Z_{1.cdq0} - HZ_{2.1dq0} - \dot{Z}_{2.1dq0}^{*}$$

$$= F_{1}u - F_{1}Z_{1.cdq0} - HZ_{2.1dq0} - \frac{\partial Z_{2.1dq0}^{*}}{\partial Z_{1.cdq0}} \frac{\partial Z_{1.cdq0}}{\partial t} - \frac{\partial Z_{2.1dq0}^{*}}{\partial \dot{Z}_{1.cdq0}^{*}} \frac{\partial^{2} Z_{1.cdq0}^{*}}{\partial t^{2}}$$

$$= F_{1}u - F_{1}Z_{1.cdq0} - HZ_{2.1dq0} - \frac{\partial Z_{2.1dq0}^{*}}{\partial Z_{1.cdq0}} \left(G_{1}\dot{i}_{dq0} - G_{1}Z_{2.1dq0} + HZ_{1.cdq0}\right) - \frac{\partial Z_{2.1dq0}^{*}}{\partial \dot{Z}_{1.cdq0}^{*}} \ddot{Z}_{1.cdq0}^{*}$$

$$(16)$$

where $u = \begin{bmatrix} V_{de} & V_{qe} & V_0 \end{bmatrix}^T$

The control law can be designed as

$$u = F_1^{-1} \left[KE + F_1 Z_{1.cdq0} + H Z_{2.1dq0} + \frac{\partial Z_{2.1dq0}^*}{\partial Z_{1.cdq0}} \left(G_1 i_{dq0} - G_1 Z_{2.1dq0} + H Z_{1.cdq0} \right) + \frac{\partial Z_{2.1dq0}^*}{\partial \dot{Z}_{1.cdq0}^*} \ddot{Z}_{1.cdq0}^* \right]$$
(17)

Putting (17) into (16) yields:

$$\dot{E}_2 = KE \tag{18}$$

where $E = \begin{bmatrix} E_1 & E_2 \end{bmatrix}^T$, $K = \begin{bmatrix} k_1 G_1^{-1} & K_2 \end{bmatrix}$ and $K_2 = \begin{bmatrix} k_{11} & 0 & 0 \\ 0 & k_{22} & 0 \\ 0 & 0 & k_{33} \end{bmatrix}$

The new error system can be represented as

$$\begin{cases} \dot{E}_1 = -G_1 E_2 \\ \dot{E}_2 = KE \end{cases}$$
(19)

Equation (19) can be rewritten as

$$\dot{E} = AE$$
(20)
where $A = \begin{bmatrix} 0 & -G_1 \\ k_1 G_1^{-1} & -K_2 \end{bmatrix}$

The characteristic equation of the system is expressed as

$$|sI - A| = \begin{bmatrix} sI & G_1 \\ -k_1G_1^{-1} & sI + K_2 \end{bmatrix} = Is^2 + K_2s + k_1I = 0$$
(21)

All the roots of (21) have a negative real part, so the coefficient matrix A of the system is a Hurwitz matrix, and the system must be stable.

The matrix P is defined to be definitely positive and the matrix $Q = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ must

satisfy the following equation as

$$A^T P + PA = -Q \tag{22}$$

The whole system Lyapunov function is given by

$$V = \frac{1}{2}E^{T}PE$$
(23)

The derivative of V along the trajectory is expressed as

$$\dot{V} = \frac{1}{2} \left(\dot{E}^T P E + E^T P \dot{E} \right)$$

$$= \frac{1}{2} E^T \left(A^T P + P A \right) E$$

$$= -\frac{1}{2} E^T Q E < 0, \quad \forall E \neq 0$$
(24)

By using the control law in (17), the converter system (9) and (10) has stability at the equilibrium E = 0.

As backstepping obtains the goals of stabilization and tracking, the final control law can be achieved by replacing F_1 , H, G_1 , ω , K and E into (17).



Figure 2. Block diagram of the proposed DVR control scheme.

Figure 2 shows the block diagram of the proposed controller, in which the dq0-axis load voltages are controlled by using backstepping control. The outputs of controller (v_a^*, v_b^*, v_c^*) are applied for SVPWM-3D (space vector pulse-width modulation –three dimensions) [15].

4. SIMULATION RESULTS

PSIM simulations have been performed for the balanced/unbalanced and linear/nonlinear loads in order to verify the feasibility of the proposed method. The DC-link voltage at the input of inverter from a three-phase AC source is 400 V, the switching frequency of inverter is 10 kHz. The filter inductor L_f is 1 mH and the filter capacitor C_f is 100 μ F. The grid voltage is 220 $V_{peak}/60$ Hz. The parameters of loads and controllers are shown in the Table 1 and Table 2, respectively.

The simulation for the PI control and proposed control method (backstepping control) under the conditions of grid voltage sags and different loads are shown from Figure 3 to 6, respectively. The grid fault is assumed to be unbalanced voltage sags, in which voltages of phases a, b, and c drop to 25%, 50% and 40%, respectively for 40 ms (from 1.53 to 1.57 seconds). During the voltage sags, when the DVR is activated, the output voltages of the DVR are injected and load voltages should be kept unchanged, as if before pre-sag. Thus, the load voltages after the sag must be much sinusoidal and balanced.

Type of load	Parameters		
Balanced linear load	$R_a=R_b=R_c=10\;\Omega$		
Unbalanced linear load	$R_a = 1 \text{ k} \Omega, R_b = R_c = 10 \Omega$		
Balanced nonlinear load	$\begin{split} L &= 1 \text{ mH, } C = 4700 \mu\text{F}, \\ R_{dca} &= R_{dcb} = R_{dcc} = 20 \Omega \end{split}$		
Unbalanced nonlinear load	$\begin{split} L &= 3 \text{ mH}, \text{C} = 4700 \mu\text{F}, \\ R_{dca} &= 100 \Omega, R_{dcb} = R_{dcc} = 20 \Omega \end{split}$		

Table 1. Parameters of loads

Controller type		Gains of controller		
PI control	Current controller	$k_p = 17.2$		
		$k_i = 13200$		
	Voltage controller	$k_{pv} = 0.32$		
		$k_{iv} = 891$		
Proposed control		$k_{11} \!= k_{22} \!= k_{33} \!= \! 2.1 \!\!\times \!\! 10^3, k_1 \!= \! 0.5 \times 10^9$		

4.1. Grid voltage sags and balanced linear loads

Figure 3A shows the performance of the DVR with the PI control under the conditions of grid voltage sags and linear loads. The DVR output voltage, load voltage, and load currents are shown in Figures 3A (b), (c), and (d), respectively. As can be seen, load voltage is sinusoidal but still has some ripples. It is demonstrated from Figures 3A (e) to (g) that, the measured values of the DVR voltage components in dq0 axis follow their references.

In the same simulation conditions, the control performance of the DVR with the proposed method is shown in Figure 3B. Figure 3B (c) shows the load voltages, which are kept at rated values even though the grid voltages drop, as shown in Figure 3B (a). The output voltages of the DVR to compensate for the voltage sags are shown in Figure 3B (b). It is illustrated in Figures 3B (e)-(g) that, the actual values of the dq0 axis DVR voltage components with the proposed strategy track their references well, respectively, which are much better than those of the PI ones (see in Figure 3B). Compared with the PI controller, the total harmonic distortion (THD) analysis for load voltage in the proposed controller gives better results with lower THD (see in Table 3).



Figure 3. Dynamic responses under the conditions of grid voltage sags and linear loads using two controllers: (A) PI controller and (B) Proposed controller.

4.2. Grid voltage sags and unbalanced linear loads

Figures 4A and 4B show the performance of the DVR with both PI and proposed controllers under the conditions of grid voltage sags and unbalanced linear loads, respectively. As can be seen clearly, the DVR output voltages in two controllers are shown in Figures 4A

(b) and 4B (b), respectively. The waveform of the load currents in both cases is unbalanced due to the influence of the unbalanced load ($R_a = 1 \text{ k } \Omega$, $R_b = R_c = 10 \Omega$), as shown in Figures 4A (d) and 4B (d). It is realized shows that the PI control method did not respond well. The load currents are illustrated in Figures 4A (d) and 4B (d). The actual values of the dq0 axis DVR voltage components in both controllers are shown from Figures 4A and 4B (e) to (g), respectively. As can be obviously seen from Figures 4B (e) to (g), the actual values of the dq0 axis DVR voltage components in the proposed controller can track their references well, compared with those of the PI one. Also, the proposed controller gives lower THD for load voltage (Figure 4B (c)) which is listed in Table 3.



Figure 4. Dynamic responses under the conditions of grid voltage sags and nonlinear loads using two controllers: (A) PI controller and (B) Proposed controller.

4.3. Grid voltage sags and balanced nonlinear loads

Figures 5A and 5B show the performance of the DVR with both PI and proposed controllers under the conditions of grid voltage sags and balanced nonlinear loads, respectively. The output

voltages of the DVR in two controllers are illustrated in Figures 5A (b) and 5B (b), respectively. The waveform of the load currents is distorted due to the influence of the nonlinear load (see Figures 5A(d) and 5B(d)). For this reason, the performance of the PI control method did not respond well. As can be seen, the actual values of the dq0 axis DVR voltage components in the proposed controller which are shown from Figures 5B (e) to (g), respectively, follow their references well, compared with those of the PI one. Also, the proposed controller gives lower THD for load voltage (Figure 5B (c)) which is shown in Table 3.



Figure 5. Dynamic response under the conditions of grid voltage sags and balanced nonlinear loads using two controllers: (A) PI controller and (B) Proposed controller.

4.4. Grid voltage sags and unbalanced nonlinear loads

Figure 6A shown the performance of the DVR with the PI control under the conditions of grid voltage sags and unbalanced nonlinear loads. The DVR output voltage is shown in Figure 6A (b) and the load voltage is sinusoidal but still has some ripple, as shown in Figure



6A (c). The load currents are illustrated in Figure 6A (d). It is illustrated from Figure 6A (e) to (g) that, the actual values of the dq0 axis DVR voltage components track their references.

Figure 6. Dynamic responses under the conditions of grid voltage sags and unbalanced nonlinear loads using two controllers: (A) PI controller and (B) Proposed controller.

Under the same simulation conditions, the control performance of the DVR with the proposed method is shown in Figure 6B. Figure 6B (c) shows the load voltages, which are kept at nominal values even though the grid voltages drop, as shown in Figure 6B (a). The output voltages of the DVR to compensate for the voltage sags are shown in Figure 6B (b). It is illustrated in Figure 6B (e)–(g) that, the actual values of the dq0 axis DVR voltage components with the proposed strategy track their references well, respectively, which are much better than those of the PI one, as shown in Figure 6B. In comparison with the PI controller, the THD

analysis for load voltage is shown in Table 3, in which the proposed controller gives better results with lower THD.

	THD (%)							
Controller type	PI control			Proposed control				
<i>•</i> • •	Phase A	Phase B	Phase C	Phase A	Phase B	Phase C		
Balanced linear load	2.37	1.70	2.15	2.19	1.24	1.81		
Unbalanced linear load	2.36	1.69	2.11	2.18	1.23	1.81		
Balanced nonlinear load	2.53	2.08	2.33	2.40	1.40	1.92		
Unbalanced nonlinear load	2.44	2.24	2.75	2.23	1.33	1.84		

Table 3. Comparison of THD of three-phase load voltages using PI and proposed controllers

5. CONCLUSION

The paper proposed a novel voltage control of three-phase four-wire DVR based on the backstepping technique. The effectiveness of the proposed control strategy was verified through simulation tests, where the load voltage is almost sinusoidal and in-phase with the soure voltage even under the conditions of grid voltage sags and different types of loads (balanced/unbalanced linear load, balanced/unbalanced nonlinear load). The feasibility of the proposed control is verified by simulation results, which show the better performance than the PI method. Also, with the proposed scheme, three-phase four-wire dynamic voltage restorers (DVR) can be extended to apply for both unbalanced and distorted source voltages effectively in the upcoming research.

REFERENCES

- 1. Khalifa Al H., Thanh Hai N., Naji Al S. An improved control strategy of 3P4W DVR systems under unbalanced and distorted voltage conditions, Electrical Power and Energy Systems **98** (2018) 233-242.
- 2. Babaei E., Kangarlu M. F., and Sabahi M. Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters, IEEE Transactions on Power Electronics **25** (4) (2010) 2676-2683.
- 3. Xu H., Ma X., and Sun D.- Reactive current assignment and control for DFIG based wind turbines during grid voltage sag and swell conditions, Journal of Power Electronics **15** (1) (2015) 235-245.
- 4. Khadkikar V. and Chandra A. UPQC-S: a novel concept of simultaneous voltage sag/swell and load reactive power compensations utilizing series inverter of UPQC, IEEE Transactions on Power Electronics **26** (9) (2011) 2414-2425.
- Kim H. and Sul S.-K. Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme, IEEE Transactions on Power Electronics 20 (5) (2005) 1169-1177.
- 6. Jimichi T., Fujita H., and Akagi H. Design and experimentation of a dynamic voltage r storer capable of significantly reducing an energy-storage element, IEEE Transactions on Industry Applications **44** (3) (2008) 817-825.

- 7. Meyer C., De Doncker R. W., Li Y. W., and Blaabjerg F. Optimized control strategy for a medium-voltage DVR theoretical investigations and experimental results, IEEE Transactions on Power Electronics **23** (6) (2008) 2746-2754.
- 8. Lee S., Chae Y., Cho J., Choe G., Mok H., and Jang D. A new control strategy for instantaneous voltage compensator using 3-phase PWM inverter, 29th Annual IEEE Power Electronics Specialists Conference (1998) 248-254.
- 9. Trinh Q.-N. and Lee H.-H. Improvement of unified power quality conditioner performance with enhanced resonant control strategy, IET Generation Transmission Distribution **8** (12) (2014) 2114-2123.
- 10. Kim D-E, Lee D-C. Feedback linearization control of three-phase UPS inverter system. IEEE Transactions on Industrial Electronics **57** (3) (2010) 963-968.
- 11. Jeong S.Y., Nguyen T.H., Le Q.A., Lee D.-C. High-performance control of three-phase four-wire DVR systems using feedback linearization, Journal of Power Electronics **16** (1) (2016) 351-361.
- 12. Van T.L., N. Nguyen M.D., L.T. Toi and T.T. Trang Advanced control strategy of dynamic voltage restorers for distribution system using sliding mode control input-ouput feedback linearization, Lecture Notes in Electrical Engineering **465** (2017) 521-531.
- 13. Van T.L., Nguyen T.H., Ho N.M., Doan X.N., and Nguyen T.H. Voltage compensation scheme for dfig wind turbine system to enhance low voltage ride-through capability, 10th International Conference on Power Electronics (ECCE Asia) (2019) 1334-1338.
- 14. Slotine J.-J. E. and Li W. Applied nonlinear control, Englewood Cliffs, NJ: Prentice-Hall (1991) 207-271.
- 15. Zhan C., Arulampalam A., Jenkins N. Four-wire dynamic voltage restorer based on a three dimensional voltage space vector PWM algorithm, IEEE on Transactions on Power Electronics **18** (4) (2003) 1093-1102.

TÓM TẮT

ĐIỀU KHIỂN PHI TUYẾN BỘ LƯU TRỮ ĐIỆN ÁP ĐỘNG BA PHA BỐN DÂY TRONG TRƯỜNG HỢP SỤT ÁP LƯỚI

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Trong bài báo này, một chiến lược điều khiển phi tuyến dùng kỹ thuật điều khiển cuốn chiếu (backstepping) cho bộ lưu trữ điện áp động (DVR) được để xuất để giảm thiểu nhiễu điện áp cho tải trong trường hợp sụt áp lưới. Mô hình phi tuyến của hệ thống với bộ nghịch lưu nguồn áp (VSI) điều chế độ rộng xung (PWM) bao gồm các bộ lọc điện cảm-tụ điện (LC) lắp đặt ở ngõ ra được xây dựng trong hệ tọa độ quay dq0. Bộ điều khiển điện áp tải theo phương dq0 được thiết kế theo lý thuyết điều khiển phi tuyến. Với chiến lược đề xuất, điện áp tải được điều khiển để đạt giá trị định mức và dạng sóng điện áp của tải gần như trở thành hình sin, so với việc dùng bộ điều khiển tích phân tỷ lệ (PI) trong trường hợp sụt áp lưới. Mô phỏng được thực hiện để kiểm chứng tính khả thi của phương pháp đề xuất.

Từ khóa: Tải phi tuyến, bộ nghịch lưu ba pha, điều khiển cuốn chiếu, tải không cân bằng.