THE DESIGN OF ALL-OPTICAL NOT AND OR GATES BASED ON 2×1 MMI COUPLERS ON AN SOI PLATFORM

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ABSTRACT

In this paper, a general theory for designing optical logic gates based on 2x1 multimode interference (MMI) structures is presented. Designs for a set of optical logic gates using silicon on insulator (SOI) channel waveguide structures are proposed and optimised. It is shown that this single structure can be used to implement a variety of optical logic and other functions. These devices are optimised by the three dimensional propagation method (3D-BPM).

Keyword. optical logic gates, silicon on insulator, optical devices, multimode interference couplers.

1. INTRODUCTION

All-optical logic gates have received considerable attention over the last couple of years. Optical logic gates have many possible applications in optical signal processing systems. Examples of potential applications include adders, subtractors, header recognizers, parity checkers, and encryption systems. There is a great need for implementing all-optical logic gates having small size, low power consumption and high-speed [1, 2]. There are many existing approaches for realizing optical logic gates. Many materials and devices have been suggested for use in optical logic. So far, optical logic schemes have been mainly based on nonlinear materials [3, 4]. The disadvantage of these approaches is that high optical powers are needed in order to obtain a nonlinear interaction. In addition, since the nonlinear coefficient is often small, long interaction lengths are generally required. Moreover, devices based on nonlinear effects are not always suitable for circuit integration. Another disadvantage is that nonlinear materials are usually expensive. Several different optical logic gates have been designed based on this nonlinear interaction principle. Yabu et al. have proposed a method for making optical logic gates by using a nonlinear material as a phase shifter in a Mach-Zehnder interferometer [5]. Using this type of device, Yabu et al. demonstrated the Boolean functions NOT and AND. Also, several other examples of nonlinear optical logic devices have been presented in the literature [6 - 10].

A second approach for realizing optical logic is to use semiconductor optical amplifiers (SOAs). SOAs are devices that amplify an optical signal without the use of optical-electrical-optical conversion [11]. Amplification is achieved in materials that exhibit optical gain. Materials such as erbium-doped silica and erbium-doped silicon as well as III-V semiconductors

can exhibit optical gain at a given wavelength when an electron population inversion is created by photons at a higher-energy pump wavelength. SOAs may be used in a number of ways to create all-optical switches and logic gates [12]. These devices all exploit the nonlinear properties of an SOA.

Recently, we have shown a general theory for realizing optical logic gates using MMI couplers [13]. In this paper, we will show the detail design for all-optical NOT and OR gates based on 2 × 1 MMI couplers on the SOI platform. The designs for these devices are optimized by the 3D-BPM method. In addition, an analysis of fabrication tolerance is also presented.

2. THEORY FOR THE DESIGN OF ALL-OPTICAL LOGIC GATES BASED ON MMI STRUCTURES

Optical logic functions can be realized using the interference between two signals. The principle of interference between two waves was first introduced by Young in the study of light [14]. If two signals having the same polarization, the same normalized amplitude but different phases φ_1 and φ_2 respectively, interfere with each other, the normalized power of the summed signal is [13]

$$P \propto \cos^2[(\varphi_1 - \varphi_2)/2] \tag{1}$$

Figure 1 shows the normalized power of the summed signal depending on the phase difference between the two signals.
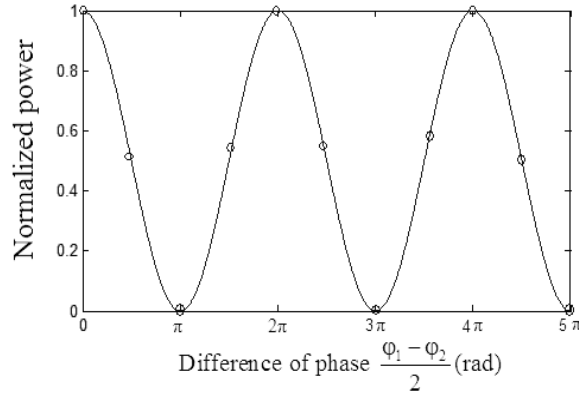

Figure 1. Normalized power of the resulting signal of the two interfering signals

It can be seen from Fig. 1 that the normalized power of the summed signal will become zero if the phases φ_1 and φ_2 satisfy the relation $\varphi_1 - \varphi_2 = \pi, 3\pi,\ldots,(2n + 1)\pi$, where n is an integer. Note that MMI structures naturally rely on interference for their operation. Therefore, optical logic gates can be realized by solely using an MMI coupler along with phase controllers and amplitude adjusters. For optical logic gates based on the MMI principle, information is encoded at the input and the output in amplitude or in phase. In this paper, only amplitude encoding of information will be used. The amplitudes and phases of input signals can be

changed so that when they are combined in an MMI structure, the output can be determined by measuring the power in output waveguides. Ideally, logic "1" is represented by $1e^{j0}$ and logic "0" is represented by $0e^{j0}$. To determine the logic level at the output of the device, the power in the output waveguide needs to be compared to a threshold value. This can be done electronically by connecting output ports to a photo-detector and a decision circuit. Another approach is to use an optical threshold device based on active MMI couplers instead of using an electronic threshold device [15]. By using the interference principle, a single MMI coupler easily performs a number of basic logic operations.

3. SIMULATIONS AND DISCUSSIONS

In this section, the optimal design for optical logic gates based on 2×1 MMI couplers is presented. The waveguide structure used in the designs is shown in Fig. 2. Here, SiO_2 ($n_{SiO_2} = 1.46$) is used as the upper cladding material. The silicon core thickness is $h_{co} = 220nm$ and the single mode waveguide width is $W_a = 480nm$. It is assumed that the designs are for the TE polarization at a central optical wavelength $\lambda = 1550nm$.
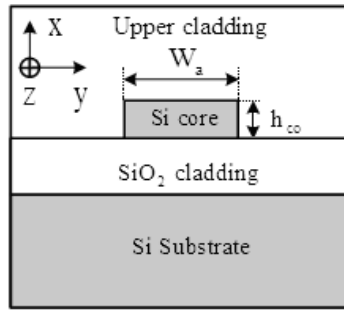

Figure 2. Waveguide cross-section used for the device design

It is well-known that widening the access waveguides improves the performance of devices. It will be shown that they can be widened via a taper from a width of $W_a = 0.48 \, \mu m$ to width W_{tp}. However, in order to reduce the width of the MMI region, the final tapered waveguide width W_{tp} still needs to be kept as small as possible. Our 3D-BPM simulations show that W_{tp} in the range $0.8 \, \mu m$ to $1.2 \, \mu m$ is sufficient to achieve the lowest loss. Adiabatic, linear and parabolic taper profiles can be used for the tapered waveguides. However, the 3D-BPM simulations show that the losses of a tapered waveguide having a length of 5 μm are nearly the same for all three cases. The loss for a linear taper of length 5 μm is 0.02 dB. Therefore, a linear taper is chosen in our designs. The designs of the tapers were carried out using the 3D-BPM with perfectly matched layer (PML) boundary conditions [16]. Figure 3 shows a top view of the light distribution along the taper for the chosen length of 5 μm, as calculated using the 3D-BPM.
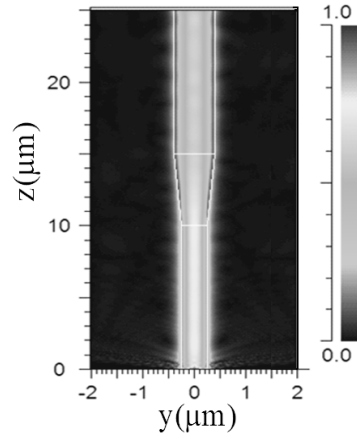
Figure 3. Power distribution along a taper length of 5 μm

Once the dimensions of the taper are known, the separation between the access waveguides can be determined. In order to achieve a compact device, the separation has to be kept as low as possible. At the same time, this separation needs to be large enough to limit, to an acceptable level, the coupling of power between the parallel adjacent input waveguides, and similarly between the output waveguides. The two parallel tapered waveguides act as a directional coupler, and thus some power may be transferred between them. Since the taper has been designed to be adiabatic, at each point along it, effectively only the fundamental local normal mode carries power. This means that the power coupling between the two tapered waveguides may be estimated as the coupling between their fundamental modes. An upper bound can be determined by calculating the coupling that takes place between two sets of two straight parallel waveguides whose widths are equal to the maximum width of the taper as shown in Fig. 4. Figure 5 shows BPM plots of the power distributions and the powers as functions of distances in two parallel waveguides having a separation of s = 400 nm. The coupling length L_c in this case is 430 μm.
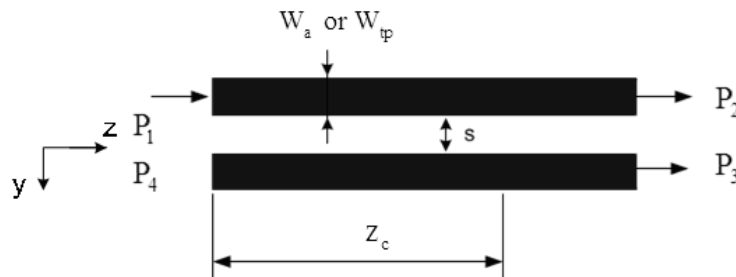

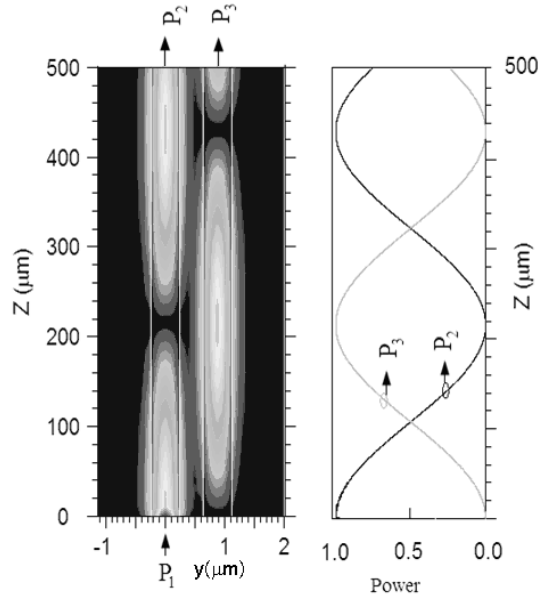*Figure 4.* Two adjacent waveguides forming a directional coupler

Figure 5. Power distribution inside the input access waveguides and the normalized powers at these waveguides for different coupling lengths

The crosstalk (i.e, the power coupling between the adjacent access waveguides) in dB is given by

$$\text{Crosstalk} = 10\log_{10}(\frac{P_4}{P_1}) \ \ (\text{dB}) \qquad\qquad (2)$$

For good isolation between the waveguides, the maximum length of the parallel waveguides needs to be determined such that it would yield a crosstalk < -30 dB. On the other hand, for rough calculations, the power coupling ratio between two parallel waveguides can be determined approximately by [17]

$$|\kappa| = \frac{\pi}{2L_c} \qquad\qquad (3)$$

where L_c is the coupling length of the directional coupler.

Equation (3) can be used for approximately determining the coupling length where the crosstalk less than -30 dB is achieved. For accurate calculations, the 3D-BPM method is used. 3D-BPM calculations show that in order to keep the crosstalk below   -30 dB at lengths $z = z_c = 10\ \mu m$ and $z = z_c = 20\ \mu m$, separations must be at least   400 nm and 500 nm, respectively.

Now consider a 2×1 MMI coupler having a minimum width of 3 µm and an optimised length of 8.3 µm using an SOI channel waveguide structure. The 3D-BPM simulation results are presented in Figs. 6(a) and 6(b).
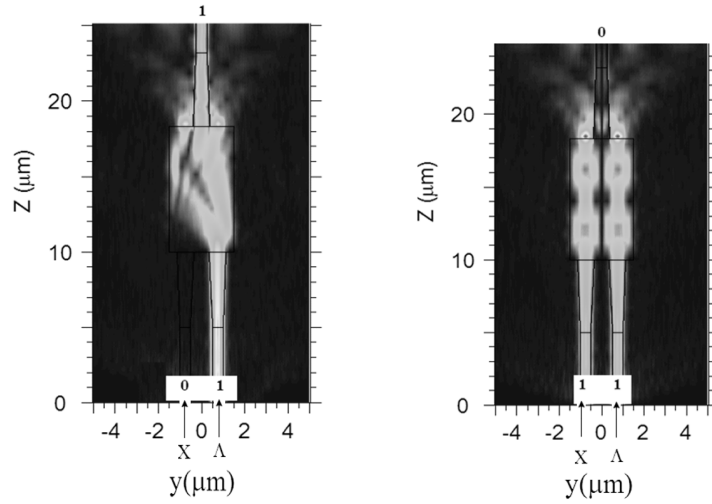
(a) Input "0-1" (b) Input "1-1"

Figure 6. A 2×1 MMI coupler as a NOT gate (a) is a demonstration of the input case
$X = 0, \Lambda = 1$ (or "0-1") and (b) is a demonstration of the input case $X = 1, \Lambda = 1$ (or "1-1").
The signal is encoded in amplitude

All incident light beams with the same wavelength ($\lambda = 1.55$ μm) and polarization are used in the simulations. An input light beam represented by the Boolean variable, X, having binary amplitude modulation of either 0 or 1 is used as input signal. An input beam represented by the Boolean variable, Λ, having a constant amplitude and phase shift of π compared with the signal at input port 1 is used as a reference beam or control beam. It is clear that a NOT gate can be realized using this 2×1 MMI coupler if the signals are encoded in amplitude, where bit "1" is represented by non-zero amplitude and bit "0" is represented as zero amplitude.

In addition, this 2×1 MMI coupler can be thought of as a Boolean OR gate, as shown in Fig. 7. If the choice for using no power in the output waveguide as logic "0" and having power in the output waveguide as logic "1" is made, then it is easy to see how this coupler performs the logical OR operation. If light is applied to either the left or right hand-side input waveguide, then light will be present in the output waveguide. The normalized output power that is calculated by the 3D-BPM method is 0.49 for both input signals "0-1" and "1-0". For the case of input signals "1-1", the normalized output power is 1.96 (power unit). This means that a threshold normalized power value of 0.3 is enough for making a decision about the bit received at the output. The excess loss is 0.08 dB.

Note that this device can be viewed as 1×2 optical combiner and 2×1 optical splitter. Also note that input beams (including data signals and reference signals) have the same wavelength and the TE polarization in all the simulations. The information is encoded in amplitude. Only phase shifters and amplitude attenuators may be required at inputs to realize various logic functions. For inputs with arbitrary polarization, polarization splitters [18] are required to separate the polarization components which can then be operated on separately and later recombined.

It is important to realize that MMI-based logic devices rely on the manipulation of phases

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of input signals. Due to fabrication tolerances, these devices can be sensitive to phase variations. Consider an OR logic gate based on a 2×1 MMI coupler shown in Fig. 8.

(a) input "0-0"

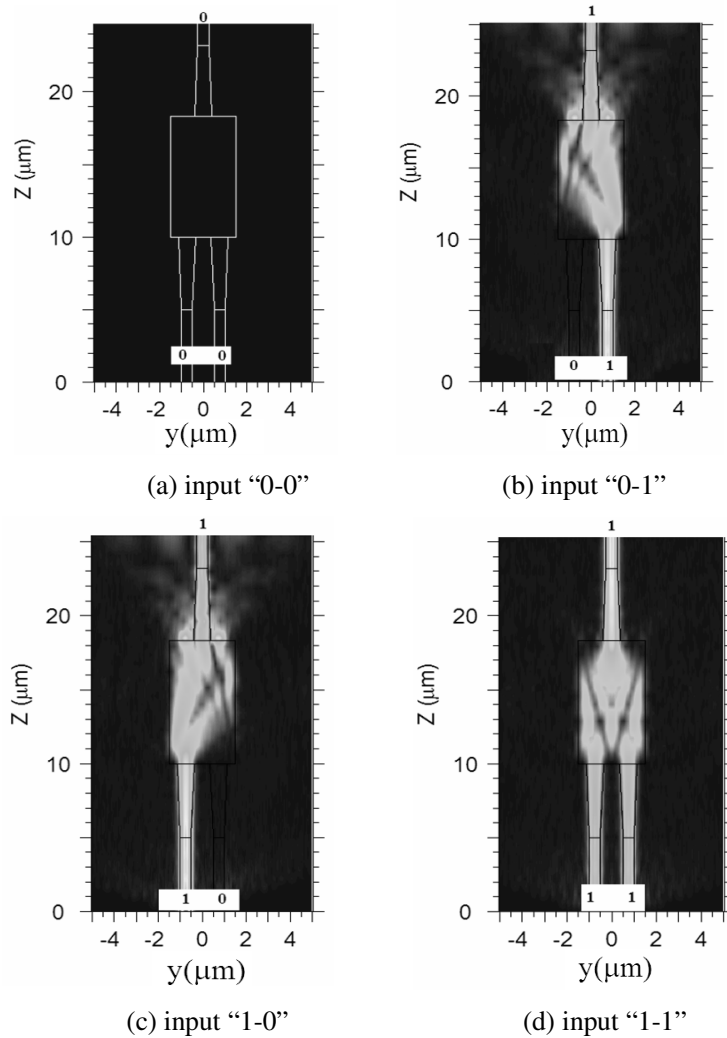(b) input "0-1"

(c) input "1-0"

(d) input "1-1"

Figure 7. A 2×1 MMI coupler as an OR gate simulated by the 3D-BPM (a) a demonstration of the "0-0" input case and (b) the "0-1" input case. (c) the "1-0" input case and (d) the "1-1" input case. The output power for cases (b) and (c) is 0.49 and for case (d) is 1.96

Figure 8. Structure of an OR logic gate based on a 2×1 SI-MMI coupler

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In order to realize the OR logic gate, the phases of the signals at input port 1 and 2 need to be identical. The effect of the phase variation $\delta\varphi$ of the input light beams on the performance of a logic gate based on a 2×1 MMI coupler is shown in Fig. 9. The 3D-BPM is used to investigate the effect of the phase difference on the performance of the device. The input light beams are: $a_1 = 1e^{j\delta\varphi}$ and $a_2 = 1e^{j0}$. Figure 9 shows the normalized output power as a function of the relative phase difference $\delta\varphi$ for four cases: (a) input signals "0-0", (b) input signals "0-1", (c) input signals "1-0" and (d) input signals "1-1".
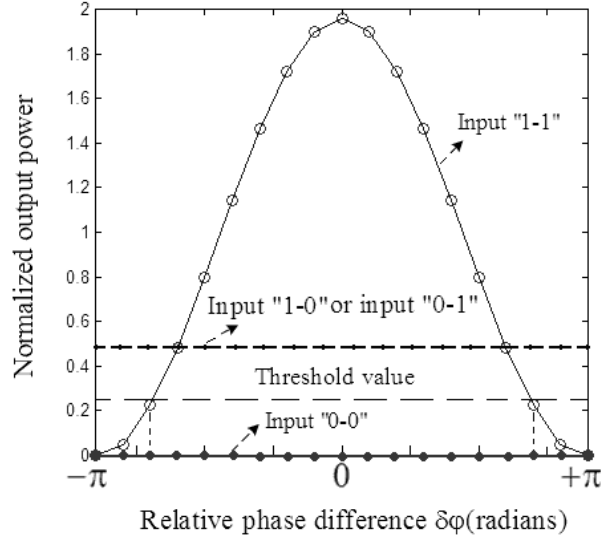

Figure 9. Normalized output power of a 2×1 MMI-based OR logic gate as a function of the phase difference $\Delta\varphi$ between two input signals

It can be seen from Fig. 5.41 that the best performance can be achieved for zero phase difference between the two input light beams. Input signals "1-0", "0-1" and "0-0" are independent of phase variations. Input signal "1-1" has a remarkable phase variation. If a normalized threshold value of 0.245 (the average value of logic "1" and logic "0") is chosen at the decision circuit, then the phase tolerance is $\delta\varphi = \pm 0.78\pi$. Therefore, the phase variation that is accommodated by one of these optical logic gates can be large. If the phase shift is implemented using multimode waveguides [19], then these relative phase tolerances are within the allowable fabrication accuracy of the order of 50 nm using existing fabrication technologies for silicon channel waveguides such as deep UV lithography or e-beam lithography.

4. CONCLUSIONS

In this paper, a theory for designing optical logic gates based on MMI structures has been proposed. Optical splitters, combiners and NOT and OR all-optical logic gates based on 2×1 MMI structures using SOI channel waveguides have been realized. The designs and fabrication tolerance analysis for these devices have been optimized using the 3D-BPM method.

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TÓM TẮT

THIẾT KẾ CÁC CỔNG LOGIC NOT VÀ OR TOÀN QUANG SỬ DỤNG THIẾT BỊ GIAO THOA ĐA MODE 2×1 TRÊN CÔNG NGHỆ SILICON

Bài báo đề xuất lí thuyết toàn cục thiết kế các cổng logic toàn quang dùng thiết bị giao thoa đa mode MMI trên công nghệ silicon. Một ví dụ về thiết kế các cổng logic toàn quang NOT và OR dùng 2×1 MMI sau đó được đưa ra. Phương pháp mô phỏng số 3D-BPM được sử dụng để tối ưu hóa việc thiết kế thiết bị và phân tích sai số chế tạo.

Từ khóa: Ống dẫn sóng quang, SOI, thiết bị đa mode MMI, cổng logic quang.

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