Model Predictive Control with Fast-computation to Balance DC-link Capacitor Voltage and Reduced Switching Frequency for 3L-NPC Rectifiers

Điều khiển dự báo nhanh bộ chỉnh lưu 3 bậc diode kẹp có cân bằng áp tụ DC và giảm tần số chuyển mạch

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Tóm tắt

Bài báo trình bày mô hình điều khiển dự báo với giải thuật tính toán nhanh kết hợp với bù delay để cân bằng điện áp tụ và giảm tần số chuyển mạch cho bộ chỉnh lưu 3 bậc diode kẹp. Đầu tiên, vector điện áp tham chiếu được thành lập từ mô hình toán của hệ thống ở dạng rời rạc. Tiếp đến, các trạng thái chuyển mạch ứng viên được chọn dựa trên vị trí vector điện áp tham chiếu. Cuối cùng, xác định được trạng thái chuyển mạch tối ưu thông qua tối thiểu hàm chi phí tổng. Qua so sánh cho thấy, phương pháp đề xuất cho kết quả điều khiển tốt hơn so với phương pháp thông thường.

Keywords

DC-link capacitor voltage balance, model predictive control, NPC rectifiers, reduce switching frequency

Abstract[1]

The paper presents model predictive control (MPC) with fast-computation combined with delay compensation to balance capacitor voltage and reduce switching frequency for the three-level (3L) diode-clamped rectifiers. First, the reference voltage vector is established from the mathematical model of the system in a discrete domain. Next, the candidate switching state vectors are selected based on the position of the reference vector. Finally, the optimal switching state is selected to minimize the global cost function. A comparative investigation shows that the proposed method gives better performance than the conventional method.

1. Introduction

Nowadays, active rectifiers are widely used in industry because of their advantages over traditional diode-based rectifiers such as bi-directional power flow, unity power factor, low total harmonic distortion (THD) of grid-side currents, and controlled DC-bus output voltage. These applications can be found in different areas, including grid-connected renewable energy systems [1], [2], energy storage systems [3], and high-voltage direct current converter station [4].

The 3L neutral-point-clamped (NPC) rectifier is often used in high-power rating, medium-voltage. Its basic circuit is shown in Fig. 1. The DC-bus output voltage is provided by two identical capacitors in series-type, and their neutral-point (NP) is connected to the mid-point of the clamping diodes in each phase. This topology generates 3 levels of voltage at the output terminal of the converter. However, its neutral point current is a main reason to cause the DC capacitor voltage imbalance. Several Pulse Width Modulation schemes have been introduced to solve this problem [5-8].

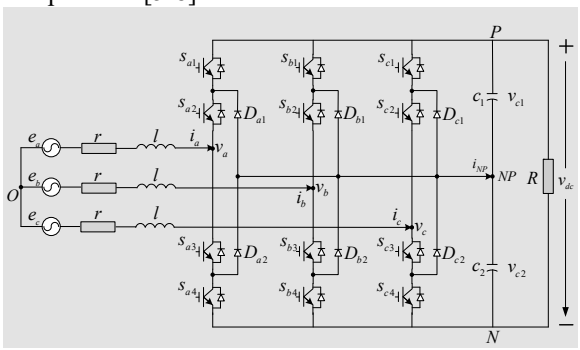

Fig. 1 *Structure of 3L-NPC rectifier system*

The carrier-based pulse-width modulation (CBPWM) method has been used to balance the DC-link capacitor voltage. It is implemented by regulating the zero-sequence component of reference voltages [5], [6]. In [7], [8], the space vector modulation (SVM) has been presented, in which the redundant switching vectors are utilized to balance the neutral-point potential. With this method, based on the

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capacitor voltage difference, one of redundant small switching vectors is selected to compensate DC voltage imbalance. These control methods require hard calculations and the relationship between the NP potential and the various switching states is very complex.

In order to keep the output voltages at the desired values under the grid voltage distortions or the load changes and unity power factor, the control algorithms such as direct power control (DPC) and voltage-oriented control (VOC) are introduced for rectifiers [9], [10]. The former control strategy is efficient, in which the active and reactive power are estimated, employing the line currents. The switching state is selected from a look-up table using the power errors. Also, the DPC scheme uses a PI-controller to generate the power reference for the inner control loop [11], [12]. However, its disadvantage is that the switching frequency is variable, and might increase the current harmonic distortion. The latter one is performed due to the orientation of the line voltage vector in synchronous rotating reference frame [13], [14]. The direct current reference is generated by DC-link voltage controller. Nevertheless, the performance depends on the quality of the current control loop and the design of parameters for PI controllers is not an easy task.

In recent years, with the development of digital signal processors, model predictive control (MPC) has been successfully applied in power electronics such as variable-speed motor drives [15], multilevel converter [16], matrix converter [17], and energy conversion systems [2]. The method is suitable for controlling fast varying electrical object, without pulse-width-modulator, fast dynamic response, and capability to compensate delay [2], [16]. However, the quality of the system response depends on the sampling frequency, which is chosen based on the minimum time required to perform all tasks [18].

In this paper, the MPC algorithm with fast-computation is proposed for a 3L- NPC rectifier with a goal of controlling three objectives: 1) to keep the DC output voltage stable even when the load or grid voltage changes, unity input power factor with sinusoidal current input; 2) to balance the DC-link capacitor voltage; 3) to reduce the switching frequency.

2. Mathematical Analysis and Modeling

The 3L-NPC rectifier scheme presented in Fig.1, each converter phase leg is composed of four IGBT switching devices and two clamping diodes. An AC input filter consisted of an inductance l and a resistance r which models the filter losses. The DC voltage of two DC-link capacitors are controlled equally (i.e., $v_{c1} = v_{c2} = v_{dc}/2$).

2.4 Circuital 3L-NPC rectifier Model

The input side of the rectifier can be modeled in the static *abc* reference frame as:

$$\begin{cases} e_a = ri_a + l\dfrac{di_a}{dt} + S_a\dfrac{v_{dc}}{2} + v_{NO} \\ e_b = ri_b + l_s\dfrac{di_b}{dt} + S_b\dfrac{v_{dc}}{2} + v_{NO} \\ e_c = ri_c + l_s\dfrac{di_c}{dt} + S_c\dfrac{v_{dc}}{2} + v_{NO} \end{cases} \quad (1)$$

Where v_{NO} is the offset voltage between the negative of DC-bus and the neutral-point of the source, and $\{\boldsymbol{S}_a, \boldsymbol{S}_b, \boldsymbol{S}_c\}$ are the switching states of NPC rectifier.

The switching state S_x is defined as shown in Figure 2: Fig. 2(a), $S_x = 2$ when two upper switches are ON while two lower switches are OFF; Fig. 2(b), $S_x = 1$ when two middle switches are ON while top and bottom switches are OFF; and Fig. 2(c), $S_x = 0$ when two upper switches are OFF while two lower switches are ON. With three modes in each phase, the converter has 27 different switching states and 19 different voltage vectors as shown in Fig. 3.

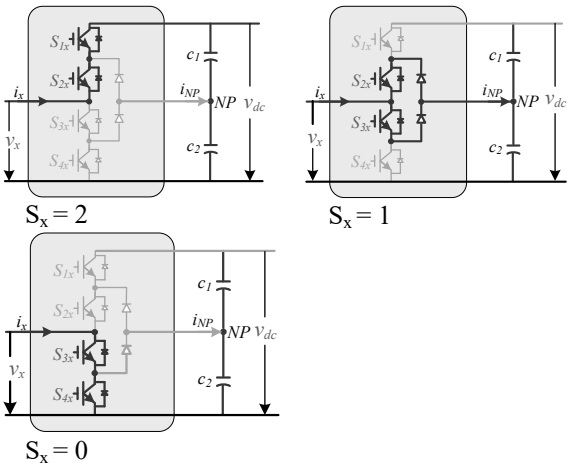


Fig. 2 *Switching state of IGBT devices per phase*

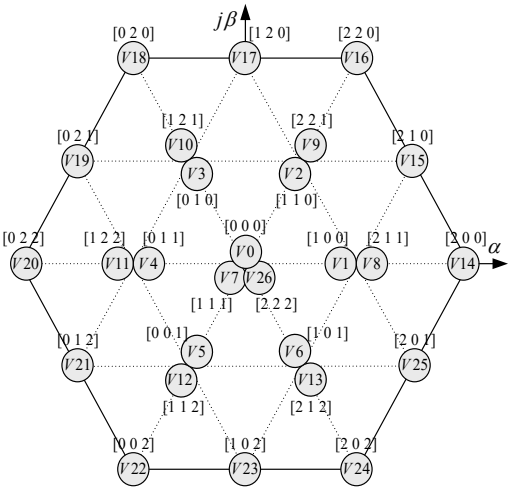


Fig. 3 *Space vector diagram for NPC rectifier*

Considering a constant DC-link voltage, and the above analyses, the voltages generated by the 3L-NPC at the rectifier terminals are showed in Table 1.

Tab. 1 *Switching states and voltages at rectifier terminals for 3L-NPC with* $x = \{a,b,c\}$

Switching Vector	Switching signals				Voltage
S_x	S_{x1}	S_{x2}	S_{x3}	S_{x4}	v_x
2	1	1	0	0	v_{dc}
1	0	1	1	0	$v_{dc}/2$
0	0	0	1	1	0

2.5 Proposed MPC

The proposed predictive control algorithm block for 3L-NPC rectifier is shown in Fig. 4. The model uses an outer linear PI controller to stabilize the DC link voltage. The DC output voltage is feedback to the controller by measuring voltages above two capacitors, the output signal of the PI controller acts as the reference current i_d^*, while the reference current i_q^* is set to 0 for unity power factor.

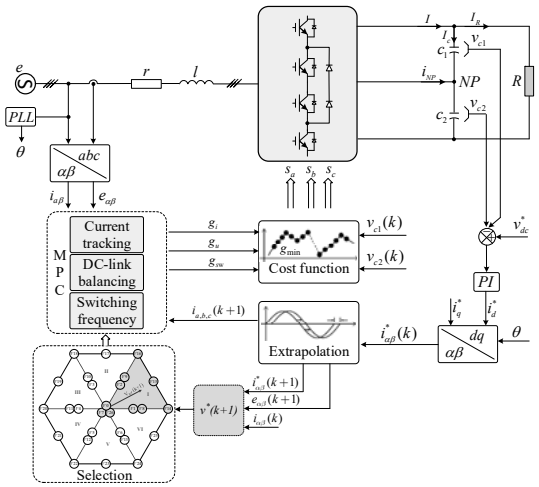


Fig. 4 *Block diagram of the proposed MPC*

The reference voltage vector at time (k+1) is calculated from the reference current, source voltage from output of the extrapolation block and measured currents at time (k). Based on the location of this vector, 10 candidate vectors were selected by Selection block to design the MPC. The MPC block is designed to current tracking, balance capacitor voltage and reduce switching frequency. The optimal switching state that minimizes the global cost function is selected.

2.6 Determine the reference voltage vector

The mathematical model of the 3L-NPC rectifier in (1) is rewritten under the αβ coordinate system as follows:

$$e_{\alpha\beta} = ri_{\alpha\beta} + l\frac{di_{\alpha\beta}}{dt} + v_{\alpha\beta} \tag{2}$$

Where $v_{\alpha\beta} = \frac{2}{3}\left(S_a + e^{j2\pi/3}S_b + e^{j4\pi/3}S_c\right)\frac{v_{dc}}{2}$ is voltage at terminals of the rectifier, S_a, S_b, and S_c are the switching states of the phases a, b, and c respectively.

The equation (2) can be obtained in discrete domain by using the Euler method with sampling period T_s as follows:

$$\frac{di}{dt} \approx \frac{i(\mathrm{k}) - i(k-1)}{T_s} \tag{3}$$

The source current in (2) can be rewritten as follow:

$$\begin{aligned} i_{\alpha\beta}(k) = i_{\alpha\beta}(k-1)&\left(\frac{l}{l+rT_s}\right) \\ &+\left(\frac{T_s}{l+rT_s}\right)\left[e_{\alpha\beta}(k) - \mathrm{v}_{\alpha\beta}(k)\right] \end{aligned} \tag{4}$$

In order to compensate delay due to algorithm calculations and analog-to-digital converters. The discrete equation of the model (4) is shifted one step forward as:

$$\begin{aligned} i_{\alpha\beta}(k+1) = i_{\alpha\beta}(k)&\left(\frac{l}{l+rT_s}\right) \\ &+\left(\frac{T_s}{l+rT_s}\right)\left[e_{\alpha\beta}(k+1) - \mathrm{v}_{\alpha\beta}(k+1)\right] \end{aligned} \tag{5}$$

According to the deadbeat control [18], the current $i_{\alpha\beta}(k+1)$ will reach its reference current $i^*_{\alpha\beta}(k+1)$ in one sampling period and can be expressed as:

$$i_{\alpha\beta}(k+1) = i^*_{\alpha\beta}(k+1) \tag{6}$$

The predicted reference voltage $v^*_{\alpha\beta}(k+1)$ at time $(k+1)$ respect to the reference current in the next sampling time can be obtained by using (5) and (6) as:

$$\begin{aligned} \mathrm{v}^*_{\alpha\beta}(k+1) = e_{\alpha\beta}(k+1) &+ \frac{l}{T_s}\mathrm{i}_{\alpha\beta}(k) \\ &-\left(r + \frac{l}{Ts}\right)\mathrm{i}^*_{\alpha\beta}(k+1) \end{aligned} \tag{7}$$

The future value of the reference current $i^*_{\alpha\beta}(k+1)$ and source voltage $e_{\alpha\beta}(k+1)$ are estimated through second-order Lagrange extrapolation, which uses one present and two past samples to calculate the future reference currents as demonstrated below:

$$i^*_{\alpha\beta}(k+1) = 3\mathrm{i}^*_{\alpha\beta}(k) - 3i^*_{\alpha\beta}(k-1) + i^*_{\alpha\beta}(k-2) \tag{8}$$

$$e_{\alpha\beta}(k+1) = 3e_{\alpha\beta}(k) - 3e_{\alpha\beta}(k-1) + e_{\alpha\beta}(k-2) \tag{9}$$

The cost function for current tracking via reference voltage vector is defined as follows:

$$g_i = \left|v^*_\alpha(k+1) - v_\alpha(k+1)\right| + \left|v^*_\beta(k+1) - v_\beta(k+1)\right| \tag{10}$$

Where $v_{\alpha\beta}(k+1)$ is voltage vector corresponding to the switching states of the 3L rectifier.

2.7 Balancing DC-link capacitor voltage

The voltage on the capacitors (v_{c1}, v_{c2}) can be calculated as follows:

$$\frac{dv_{c1}}{dt} = -\frac{1}{2C} i_{NP} \quad (11)$$

$$\frac{dv_{c2}}{dt} = \frac{1}{2C} i_{NP} \quad (12)$$

Where C_1=C_2=C is capacitance of each DC-link capacitor; i_{NP} is the current at the mid-point of DC-link capacitor Z can be defined from load currents i_a, i_b, i_c on each phase and switching state in Table 1.

$$i_z = \sum_{x=a,b,c} \text{state}(S_x) i_x \quad (13)$$

$$\text{Where state}(S_x) = \begin{cases} 1 & \text{if } \begin{cases} S_x = 1 \\ S_x = 2 \text{ or } S_x = 0 \end{cases} \\ 0 \end{cases}$$

Using Eq. (3), the voltage of each capacitor in discrete domain can be written as:

$$v_{c1}(k) = v_{c1}(k-1) - \frac{T_s}{2C} i_{NP}(k) \quad (14)$$

$$v_{c2}(k) = v_{c2}(k-1) + \frac{T_s}{2C} i_{NP}(k) \quad (15)$$

Equation (14) and (15) are shifted one step forward for the purpose of delay compensation.

$$v_{c1}(k+1) = v_{c1}(k) - \frac{T_s}{2C} i_{NP}(k+1) \quad (16)$$

$$v_{c2}(k+1) = v_{c2}(k) + \frac{T_s}{2C} i_{NP}(k+1) \quad (17)$$

The cost function for DC-link capacitor voltage balance is defined as:

$$g_{dc} = \left(v_{c1}(k+1) - v_{c2}(k+1)\right)^2 \quad (18)$$

2.8 Strategy to reduce computation time

The conventional MPC algorithm for 3-level converter needs at least 52µs to perform all the tasks [18]. At each sampling time, this solution uses all 27 switching states for the model predictive to determine the optimal state. This section presents a strategy to reduce execution time based on the position of the predicted reference voltage vector at time *(k + 1)*. The space vector can be divided into six sectors, assuming that the reference voltage vector located in sector I at the time *(k + 1)* as Fig. 5. In this sector, there are 10 nearest switching states to the reference vector that are used as candidate vectors for the prediction model. This solution significantly reduces execution time by using 10 instead of 27 switching states as in the conventional method.

With 10 switching states in each sector corresponding to the location of the reference vector can ensure the balancing of capacitor voltage or not. This issue will be clarified by the analysis below.

The voltage difference between the two capacitors is determined as follows:

$$\Delta v_c(k+1) = \left[v_{c1}(k+1) - v_{c2}(k+1)\right] - \frac{T_s}{C} i_{NP}(k+1) \quad (19)$$

From (19) indicates that the capacitor voltage balance is controlled by the current i_{NP}. When an imbalance occurs following the trend $v_{c1} > v_{c2}$, the required current is positive and negative for $v_{c1} > v_{c2}$. Otherwise, the required current to be zero if $v_{c1} = v_{c2}$.

As analyzed in Fig. 2(a), 2(c), while $S_x = 2$ or $S_x = 0$, no current flows to the mid-point of the DC-link, so $i_{NP} = 0$. In case $S_x = 1$, the current $i_{NP} = i_x$ depends on the current on the source phase with $x = \{a,b,c\}$. Similar analysis for 10 candidate voltage vectors in sector I, their effects on current i_z are listed as in Table 2. In which, there are 5 vectors for the current $i_{NP} = 0$, and 5 remaining vectors always exist at least one state for i_{NP} is either positive or negative. Therefore, they ensure the conditions for MPC algorithm to perform capacitor voltage balancing.

A similar way is repeated when analyzing for the remaining sectors. The candidate switching states for the 6 sectors are shown in the Table 3.

Tab.2 *Switching states for 6 sectors*

Switching states	Current i_{NP}	Switching states	Current i_{NP}
V0 [0 0 0]	$i_{NP} = 0$	V1 [1 0 0]	$i_{NP} = i_a$
V7 [1 1 1]	$i_{NP} = 0$	V15 [2 1 0]	$i_{NP} = i_b$
V26 [2 2 2]	$i_{NP} = 0$	V9 [2 2 1]	$i_{NP} = i_c$
V14 [2 0 0]	$i_{NP} = 0$	V2 [1 1 0]	$i_{NP} = i_a + i_b$
V16 [2 2 0]	$i_{NP} = 0$	V8 [2 1 1]	$i_{NP} = i_b + i_c$

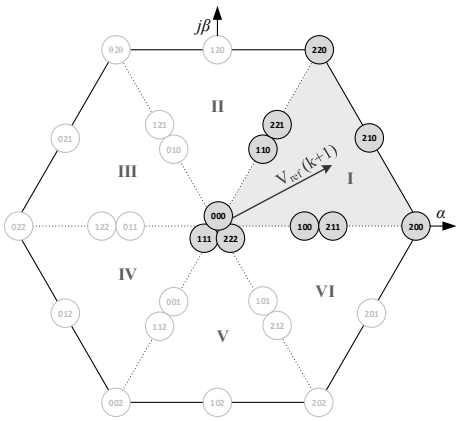


Fig. 5 *Candidate vector selection strategy for sector I*

Tab.3 *Switching states for 6 sectors*

Sector	Pre-selected voltage vectors	Sector	Pre-selected voltage vectors
I	V0, V1, V2, V7, V8, V9, V14, V15, V16, V26	IV	V0, V4, V5, V7, V11, V12, V20, V21, V22, V26
II	V0, V2, V3, V7, V9, V10, V16, V17, V18, V26	V	V0, V5, V6, V7, V12, V13, V22, V23, V24, V26
III	V0, V3, V4, V7, V10, V11, V18, V19, V20, V26	VI	V0, V1, V6, V7, V8, V13, V14, V25, V25, V26

2.9 Reduction of switching frequency

In the MPC algorithm, the performance of the control depends on the sampling time. The higher sampling frequency, the better system response. However, it also makes high switching frequency. The IGBT switching devices and drivers should operate at frequency lower than the manufacturer's recommended range. Therefore, reduction of the switching frequency is necessary.

For NPC 3 L rectifiers with 4 switches per phase leg, the cost function to minimize the number of switching between two consecutive sampling is defined as follows:

$$g_{sw} = \sum_{i=1}^{4} \sum_{x=a,b,c} \left| s_{xi}^{p}(k+1) - s_{xi}(k) \right| \quad (20)$$

Where $s_{xi}^{p}(k+1)$ and $s_{xi}(k)$ are the predicted switching states at time $(k+1)$ and switching states at time (k) of i^{th} device, respectively.

2.10 Global cost function

In this section, 3L MPC control algorithm is used to control multi-objects: current tracking, balancing the DC-link capacitor voltage and reduction of switching frequency with the global cost function is defined in the following:

$$g = g_i + \lambda_{dc} g_{dc} + \lambda_{sw} g_{sw} \quad (21)$$

Where λ_{dc} and λ_{sw} are the weighting factors to regulate the capacitors voltage and switching frequency respectively.

The adjustment of weighting factors is very important in controlling the objects to achieve the desired goal [16]. The optimal switching state is selected based on the minimized value of the global cost function.

2.11 Design of DC voltage controller

To control the DC output voltage, an outer linear PI controller is proposed as shown in Fig.6. It is assumed that the DC output voltage is constant, the transfer function between output voltage and input current through Laplace transform is written as follows:

$$I = I_c + I_R = \frac{V_{dc}}{2/Cs} + \frac{V_{dc}}{R} \quad (22)$$

$$\frac{V_{dc}}{I} = \frac{R}{RCs/2+1} \quad (23)$$

Where $C/2$ is the capacitance of two capacitors C_1 and C_2 in series; R is resistance of load.

The PI controller parameters should be properly tuned to ensure fast transient response and less steady-state errors. For a first order system, PI parameters can easily be calculated using Ziegler-Nichols method [19].

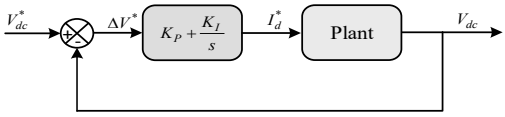


Fig. 6 *PI controller for DC voltage*

2.12 Implementation of Control Scheme

The flowchart for the digital implementation of 3L MPC algorithm with fast computation is shown in Fig. 6. consists mainly of nine steps as follows:

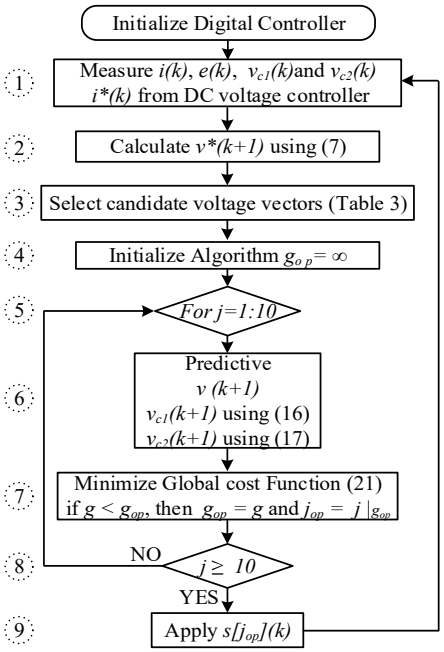


Fig. 7 *Implementation of FCS-MPC algorithm*

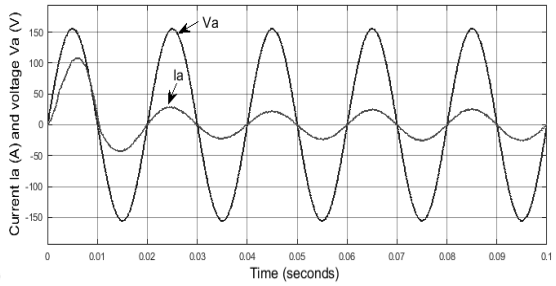
Tab.4 *System and control parameters*

Description	Variable	Value
Phase voltage source (rms)	e	110 V
Source frequency	f	50 Hz
Reference DC voltage	v_{dc}^{*}	400 V
Filter resistance	r	0.5 Ω
Filter inductance	l	4.2 mH
DC-link capacitor	C_1, C_2	3500 µF
Load resistance	R	30 Ω
Sampling period	T_s	50 µs
PI controller	k_p	0.3
	k_i	30
Weighting factor	λ_u	1
	λ_{sw}	0.2

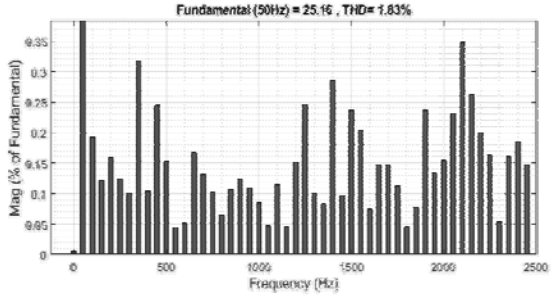
3. Simulation Results

This section presents the results of the Matlab/Simulink to verify the effectiveness of the proposed algorithm compared to conventional algorithm. The model is configured with the parameters as in the Table 4. In which, the initial voltage on upper capacitor is set to 150V and lower capacitor is 0V to generate an unbalance of the capacitor voltages.

In the first case, the simulation process is performed with changing load parameters. At time t = 0.15s, a resistive load of 30 Ω is added in parallel with the current load, and disconnected from the circuit at time t = 0.3s. As the results are shown in Fig. 8(a) and 8(b), input current has sinusoidal waveform (THD = 1.83%) and in phase with source voltage.



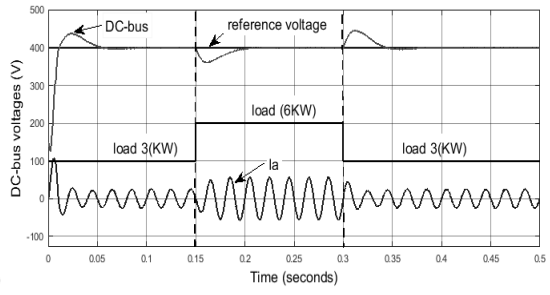
a)



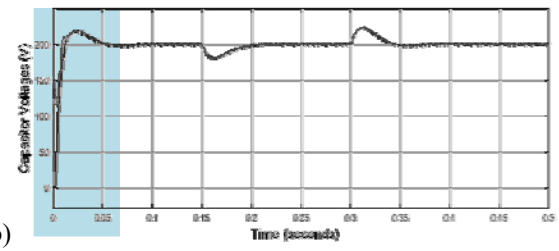
b)

Fig. 8 *Response of current and grid voltage on phase a: (a) Current and voltage; (b) Current harmonic spectrum*

The DC-bus voltage is quickly achieved at set value. Despite the transient occurs at the time of changing the load parameters with overshoot about 5% but quickly extinguished after 0.05s as Fig. 9(a). The remaining results in Fig. 9(b) and 9(c), although the capacitor voltages were set to produce an imbalance at the time t = 0, they quickly reached equilibrium after 0.01s.



a)



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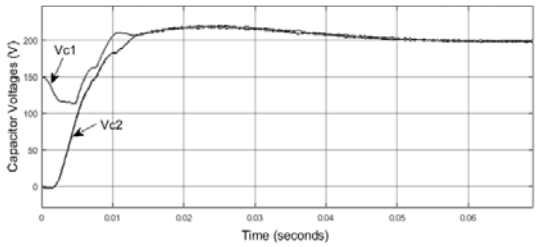
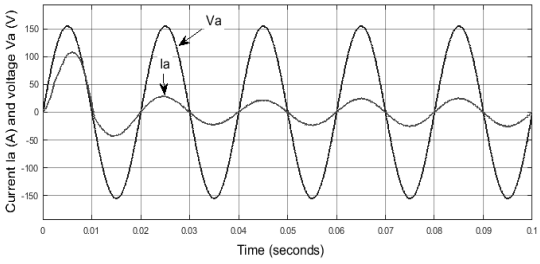


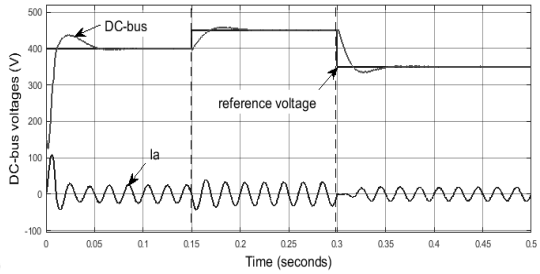
c)

Fig. 9 *Response of DC-bus and capacitor voltages: (a) DC-bus voltage; (b) Capacitor voltages; (c) The magnification of the area is highlighted*

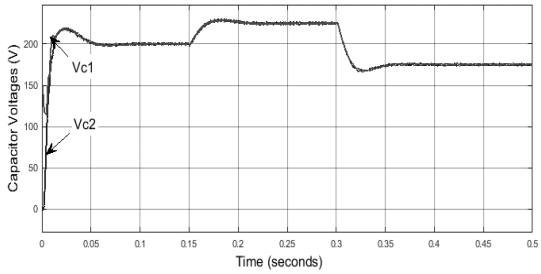
To further demonstrate the performance of the proposed method, a simulation was performed under changes of the input reference DC voltage. At time t = 0.15s, reference DC voltage changes from 400V to 450V, and from 450V back to 350V at time t = 0.3s. As observed in Figure 10, the system response is similar to the case of changing load parameters such as the unit power factor as Fig. 10(a), the DC-link voltage quickly reaches reference value in Fig. 10(b), and the capacitor voltage is balanced with a small difference of about 0.2V as shown in Figure 10 (c).



a)



b)



c)

Fig. 10 *System responses when changing the reference DC voltage: (a) Current and voltage phase a; (b) DC-bus voltage; (c) Capacitor voltages*

In order to improve the performance of the MPC algorithm, the sample time is reduced to get better results. However, this makes switching frequency higher. Therefore, reducing the switching frequency is necessary for power converters to operate within the

allowable range. A cost function to reduce the switching frequency has been proposed in this paper as in section 2.6. The evaluation of the effectiveness of this function is verified through simulations with variable weight factors λ_{sw}. The simulation is performed with a sampling frequency at 20kHz. The results are shown in Fig. 11, when increasing weight factor λ_{sw} will be reduced the switching frequency. However, it also increases the THD of the grid current and the voltage difference between capacitors.

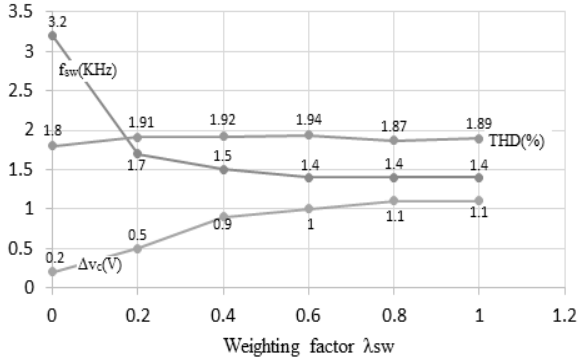


Fig. 11 *Effect of weighting factor on system response*

To obtain a fair comparison between the proposed method and the traditional method, the simulations were performed at sample time 75 µs on both with the same configuration parameters as shown in Table 4. Program execution time is measured on TI's F29379D DSP card via the Real-Time Code Execution Profiling tool. The results obtained in Table 5 show that both the proposed and conventional methods have similar effect. The proposed method improves the current THD, but balancing the capacitor voltage and reducing the switching frequency is not as good as the conventional method.

Tab.5 *Comparison result of two methods*

T_s=75 µs	Proposed MPC			Conventional MPC		
λ_{sw}	THD	Δ_{Vc}	f_{sw}	THD	Δ_{Vc}	f_{sw}
0	2.85	0.4	2.2	2.88	0.3	2.2
0.2	2.85	0.6	1.4	2.99	0.5	1.4
0.4	2.91	0.7	1.2	3.01	0.6	1.2
0.6	2.96	0.8	1.1	3.13	0.7	1
0.8	2.88	1	1	2.91	0.9	0.95
1	2.94	1	1	3.04	1	0.86
Execution time (*ns*)	48052			56821		

The best improvement is the execution time. The program execution time is shown in Figure 12, the proposed method takes about 48.052μs to complete all tasks, while the conventional method is 56.821μs. This is important in the algorithm that uses MPC, especially in multi-level converters with more switching states that need to operate at high sampling frequencies to improve system control quality. Specifically, the conventional method with 27 switching vectors per loop cycle cannot operate at 50μs sampling time, but can be performed based on the fast calculation algorithm proposed in this paper.

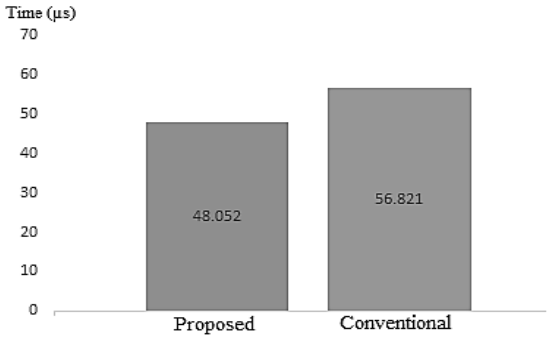


Fig. 12 *Compare execution time between proposed and conventional method*

4. Conclusions

In the paper, 3L-MPC algorithm with fast calculation is proposed to control many objectives such as unit power factor, capacitor voltage balance and switching frequency reduction. In addition, the outer PI controller is used to adjust the DC-bus voltage. The simulation results demonstrated the excellent performance of the proposed method, both in transient and steady states.

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