ENHANCE IMPEADACE SOURCE NETWORK FOR SINGLE PHASE FIVE-LEVEL DUAL BOOST T-CELL INVERTER

Thao Nguyen Duy
HCMC University of Technology and Education
Ho Chi Minh, Vietnam
thaond@hcmute.edu.vn

Hung Nguyen Tan
FPT Polytechnic
FPT University
Ho Chi Minh, Vietnam
hungnt169@fe.edu.vn

Linh Thai Hoang
HCMC University of Technology and Education
Ho Chi Minh, Vietnam
linhth@hcmute.edu.vn

Duc Tri Do
HCMC University of Technology and Education
Ho Chi Minh, Vietnam
tridd@hcmute.edu.vn

ABSTRACT

The use of mid-point-clamped multilevel inverters, such as active neutral point-clamped or stacked multicell converters, has risen significantly in recent years. This expansion can be attributed to significant voltage gains, major decreases in common-mode voltage and leakage current, enhanced bidirectional power flow capacity. However, there is a problem with the maximum AC output voltage is just half of the dc-link voltage. In order to overcome this constraint and properly handle low also widely variable input voltages, an additional front-end boost circuit must be integrated. In the present study, a single phase five-level Dual boost T-Cell inverter that may equal the peak amplitude of the grid voltage even when the dc-link voltage is low and varies considerably is explored. This paper proposes an enhance impedance source network (switch boost network) to improve the DC-link from a low-amplitude input source, allowing dynamic voltage gain also increased them. To control the proposed topology, the 1800 carrier phase shift algorithm (PS) with two carriers for a five-level topology will be used. Both the analysis and results of simulation will be illustrated as proof of the accuracy of this proposed.

Keywords: *Dual Boost T-Cell Inverter, Impedance Source Network, switch boost network, PS algorithm, dynamic voltage gain.*

1. INTRODUCTION

In recent years, high efficiency power converters have drawn significant interest in order to meet the application requirements for grid-connected renewable energy or electric vehicles [1],[2]. Multilevel inverters (MLI) are gaining popularity due to their high power conversion efficiency, low EMI for improved the lifespan, and low dv/dt,

which reduces output filter size and volume [3]. In this instance, it's common to utilize supplementary front-end dc-dc boost converters preceding MLI. These converters facilitate the transmission of power from low-capacity dc voltage sources, such as photovoltaic (PV) string arrays, to the ac/grid side [4].

Conventional MLIs are classified into several types based on their operational configuration. Many topologies have the advantage of reduce common mode voltage, decreasing leak current propagation, and voltage/current stress on semiconductor such as: Mid-Point Clamped based MLI with Active Neutral Point (ANPC) [5], Stacked-Multicell Inverter (SMC) [6], T-type Inverter [7], Flying Capacitor Inverter [8],…. However, one restriction of ANPC, T-type inverters and SMC arrangements is that they only use half of the dc-link voltage. A dc-dc boost converter is required to overcome this drawback and improve system performance. This converter serves as an essential interface, increasing the low dc-link voltage to a greater range, efficiently addressing the limited dc-link voltage use. The system is able to achieve greater effectiveness and performance, showing an opportunity for further advances and improvements in MLI. Figure 1 shows an ANPC 5-stage 1-phase inverter configuration using a front-end DC-DC converter to increase the DC-Link voltage [9]. Figure 2 depicts a 1 phase 5L-SMC inverter topology that employs a front-end DC-DC similarly to Fig 1 [6]. However, adding a traditional DC-DC converter leads to an increase in system size as well as reduced performance [10].

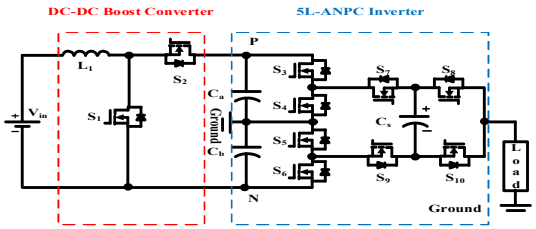

Fig. 1. *Convetional two-stage DC-DC boost 5L-ANPC inverter [9]*

The integration of the Switched Capacitor (SC) concept into conventional MLI has received much attention as an achievable choice for reducing the limits caused by the standard dc-dc boost converter located at the front of the inverter design. This method improves voltage regulation adaptability, potentially leading to more efficient and adaptive power conversion systems [11]. However, SC-networks include discontinuous input current profiles, which causes spiky current stress on the MLI switches. In addition, the voltage gain when using SC-network for input boost is also a major drawback. There has been a concerted effort to integrate the dual power processing stages of dc–dc and dc–ac conversion into a unified single-stage dc–ac converter. The objective of this integration is to improve overall system efficiency and power density. An initial approach towards this integration involves employing impedance-source (IS)-based inverters

featuring integrated shoot-through operation and a five level (5L) output voltage waveform [12]. The incorporation of shoot-through operation within IS-based inverters holds promise for enhancing operational efficiency and refining the output voltage waveform by enabling a greater number of output voltage levels. However, achieving a substantial increase in output voltage levels requires the utilization of multiple IS networks with isolated dc voltage sources, thereby introducing circuit complexity and imposing constraints on leakage current suppression.

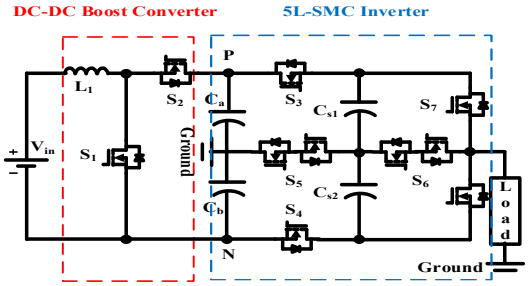

Fig. 2. *Conventional two-stage DC-DC boost 5L-SMC inverter [6]*

To overcome the shortcomings of the above studies, this study proposes a topology, 5L-Dual Boost T-Cell, which has the advantage of peak output voltage reaching the entire DC-link voltage instead of half compared to previous configurations. An enhance impedance source network (SB) is adjusted accordingly to increase the voltage gain. Theoretical analysis of operating principles and simulation results will be presented in this paper.

2. OPERATING PRINCIPLE OF 5L-SB-DBTCI

Fig.3 illustrates the propose topology of 5L-SB-DBTCI. This scheme includes a single-state boost DC-link and single-phase five-level inverter.

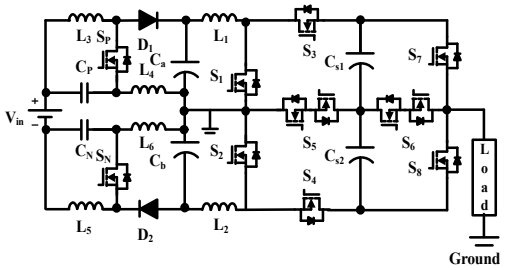

Fig. 3. *The propose topology of 5L-SB-DBTCI*

2.1 Impedance source network

This enhanced impedance source network (SBN) is made up of two symmetrical networks about the neutral point. Six inductors (L_1, L_2, L_3, L_4, L_5, L_6) charge and discharge current while also representing the characteristics of the impedance source as short circuit protection for the system, and four capacitors (C_a, C_b, C_P, C_N) accumulate and release voltage to increase DC-link voltage profile, two diodes (D_1, D_2) used to conduct direct current and two switches (S_P, S_N) to control the DC-link voltage flexibly according to the algorithm.

Based on the operating status of 5 levels - Dual boost T-Cell Inverter topology as well as the simultaneous switching and switching ratio of S_P and S_N, SBN has 3 operating states: Shoot through 1 (ST1), Shoot through 2 (ST2) and Non-Shoot through (NST). Figure 4

shows the equivalent circuits in different states of the SBN.

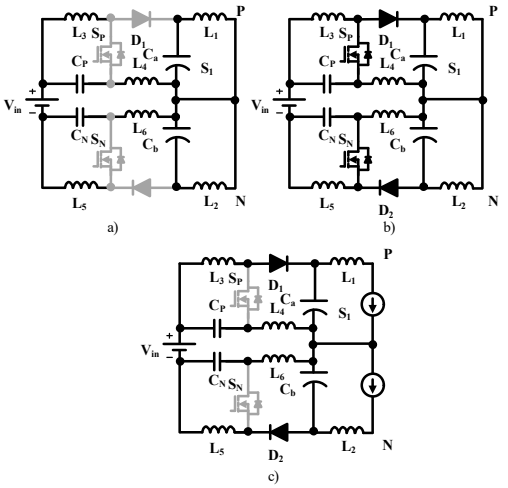

Fig. 4. *The equivalent circuit of SBN in three states (a) Shoot through 1, (b) Shoot through 2, c) Non-Shoot through*

Based on the cycle of operating states of SBN described in Figure 4, we can explain that at ST1 state, the switches on the 5L-DBTCI side are shoot through (S_1&S_2 turn on at the same time), the S_P and S_N switches turn off, leading to Diodes D_1 and D_2 reverse bias, inductors L_1, L_2 charge, L_3, L_4 remain constant, L_5, L_6 discharge, capacitors C_P, C_N C_a, C_b charge. Similarly, in ST2 state, S_P and S_N turn on, D_1 and D_2 are forward biased, inductors L_1, L_2 discharge, L_3, L_4, L_5, L_6 charge, capacitors C_P, C_N C_a, C_b charge. In NST state, SP and SN still turn off. D_1 and D_2 are forward biased. inductors and capacitors in the discharged state.

2.2 5L-Dual Boost T Cell Inverter

Based on the operating state of SBN and the control algorithm, the 5L-DBTCI topology can be analyzed into 8 operating states.

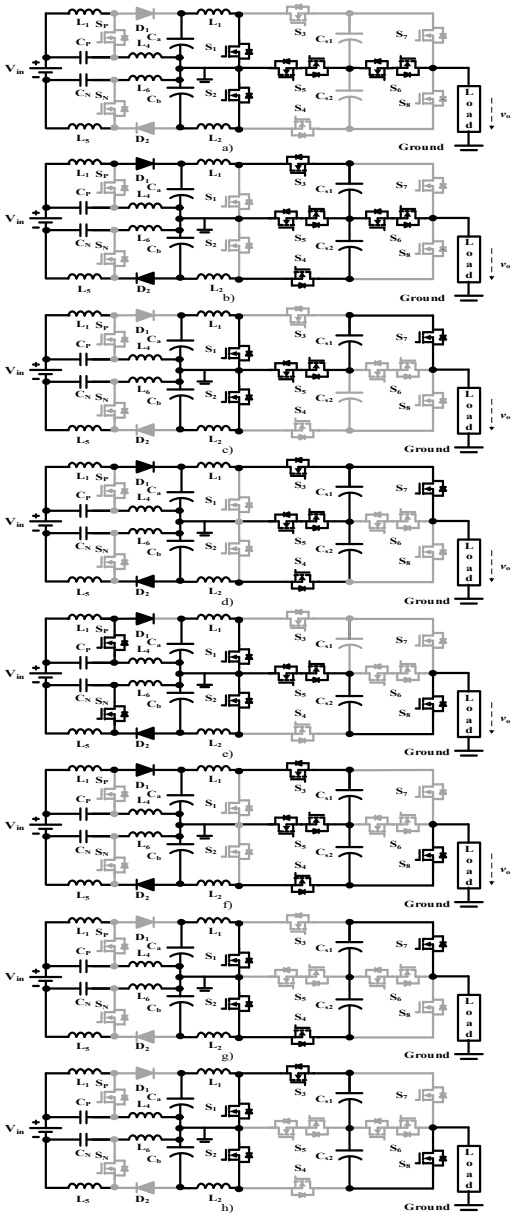

Fig. 5. *Equivalent circuits correspond to each operating state in an operating cycle of 5L-SB-DBTCI. a) v_0=0V, b) v_0=0V, c) v_0= +V_{CS1}, d) v_0= +V_{CS1}, e) v_0= +V_{CS2}, f) v_0= -V_{CS2}, g) v_0= V_{CS1}+ V_{CS2}, h) v_0= -V_{CS1}- V_{CS2}*

Figure 5 shows the topology states corresponding to each output voltage level. The state of the switches corresponding to the output voltage level is shown in Table 1 with the insertion of the S_N/S_P control interval into S_1, S_2, S_5

and S_8. It can be seen that the topology produces 5 different voltage levels related to the voltage applied on the capacitors C_{S1} and C_{S2} including: $-V_{CS1}$ - V_{CS2}, $-V_{CS2}$, 0, $+V_{CS2}$, $+V_{CS1}$ $+V_{CS2}$, . If the two capacitors C_{S1} and C_{S2} are balanced in ideal conditions, then V_{CS1} = V_{CS2}.

Based on the corresponding operating states of inductors and capacitors on the topology as well as on-off of the switches, we can calculate the DC-Link voltage as follows:

$$V_{PN} = V_{in}.\frac{2(1-d_0)}{2.\left[1-d_0(1-d_{st})\right]-5d_{st}m} \quad (1)$$

Where V_{in} is the input voltage, d_0 is the duty ratio of S_P and S_N, d_{st} is the shoot through ratio, m is the modulation index. The boost factor B is determined as follows:

$$B = \frac{V_{PN}}{V_{in}} = \frac{2\left(1-d_0\right)}{2\left[1-d_0(1-d_{st})\right]-5d_{st}m} \quad (2)$$

V_{CS1} and V_{CS2} are defined as follows:

$$V_{C_{S1}} = V_{C_{S2}} = \frac{V_{PN}}{1-2d_{st}} \quad (3)$$

The peak voltage can be calculated as follows:

$$\hat{v}_o = V_{C_{S1}} + V_{C_{S2}} = \frac{2V_{PN}}{1-2d_{st}} \quad (4)$$

The voltage gain is calculated to be determined:

$$G = \frac{\hat{v}_o}{V_{in}} \quad (5)$$

Table 1. *The switching states and the output voltage of 5L-SB-DBTCI*

Switches turn ON	***Level of Output Voltage***
S_1, S_2, S_5, S_6	0V
S_3, S_4, S_5, S_6	0V
S_1, S_2, S_5, S_7	V_{CS1}
S_3, S_4, S_5, S_7	V_{Cs1}
S_1, S_2, S_5, S_8, S_P, S_N	$-V_{CS2}$
S_3, S_4, S_5, S_8	$-V_{CS2}$
S_1, S_2, S_4, S_7	$V_{CS1}+V_{CS2}$
S_1, S_2, S_3, S_8	$-V_{CS1}-V_{CS2}$

3. PWM CONTROL SCHEME FOR THE 5L-SB-DBTCI

The gating signal waveform is shown in Fig 6 by the reference voltage of. The reference voltage function for 5L-SB-DBTCI is shown below:

In this control method, a sine-shaped reference signal with a function like equation (6) is compared with two high-frequency carriers under the condition that the carriers are 180^0 degrees apart. Together, the two signals Vcon and Vst is included to provide S_P/S_N control timing as well as shoot through to enhance voltage gain. Figure 7 shows the logic circuit used to the PS algorithm's control principle and the shoot-through insertion method.

$$v_{ref}(t) = m\sin\left(\omega t\right) \quad (6)$$

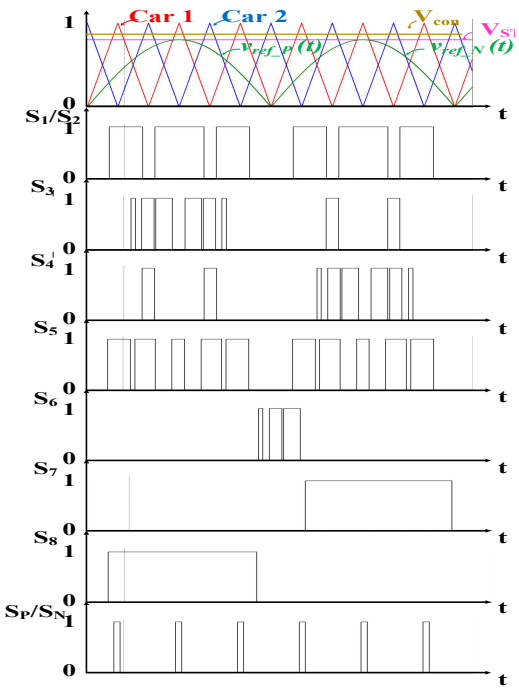

Fig. 6. *Waveforms of gating signals of control technique for the 5L-SB-DBTCI*

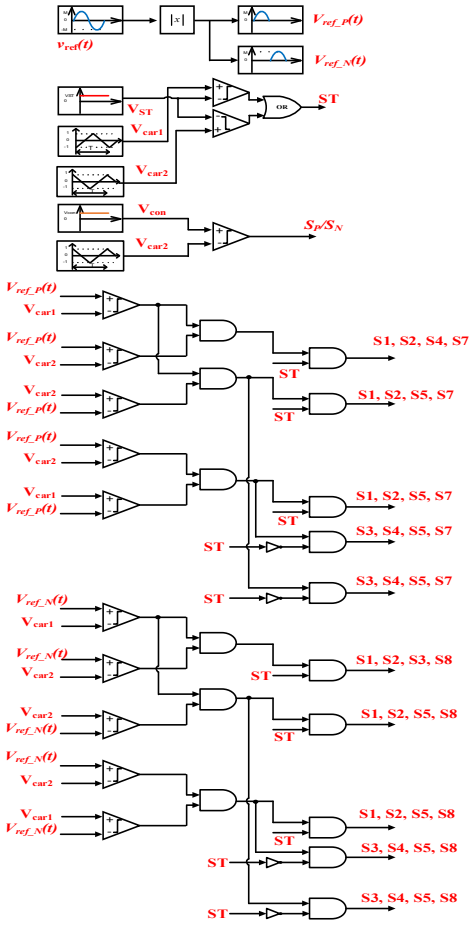

Fig. 7. *Logic circuit of control technique for the 5L-SB-DBTCI*

4. COMPARATIVE ANALISYS

To emphasize the significance of the proposed inverter, a comparison was made between the newly introduced inverter and several existing ones, specifically the 5L-ANPC and 5L-SMC topology.

The overall comparison is presented in Table II. Among these topologies, the 5L-ANPC and 5L-SMC employ a smaller number of components. In contrast, both the 5L-ANPC and 5L-SMC do not utilize active switches in an impedance-source network; instead, they incorporate two switches in the boost configuration. As indicated in Table II, the 5L-ANPC and 5L-SMC have a peak output voltage of DC-Link/2, whereas the proposed inverter operates at DC-Link. Moreover, the proposed inverter exhibits a higher voltage gain than the 5L-ANPC and 5L-SMC, along with superior shot-through immunity.

Table 2. *Overall Comparison*

	S	Bi	Caps self balacing	Peak Output Voltage	VG
5L-ANPC	10	Y	No	DC-Link/2	L
5L-SMC	10	Y	No	DC-Link/2	L
Propose topology	12	Y	Y	DC-Link	H

Switch: S; Continuous: Cont; Bidirectional: Bi; Voltage gain: G, Yes: Y; High: H; Low: L.

5. SIMULATION RESULTS

Numerous simulations were carried out using the PSIM simulation software to validate the performance of the strategy approach for the 5L-SB-DBTCI topology. The simulations were conducted with the parameters listed in Table III, allowing for a comprehensive review of the technique's operation and effectiveness.

Table 3. *Parameters used in simulation*

Parameters	***Value***
Input voltage	100V
DC-link	173V
Output voltage	$320V_{rms}$
Shoot-through ratio	0.2
d_0 ratio (S_P/S_N duty cycle)	0.1
Modulation index	0.8
Carrier frequency	10Khz
Inductance	470 μH
Capacitance	4400uF
Resistive load	40Ω

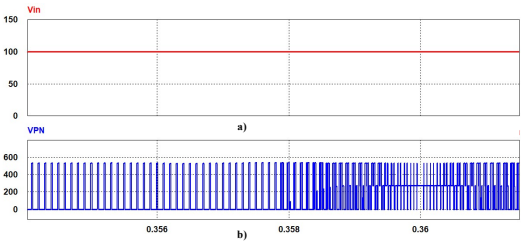

Fig. 8. *Simulation results of 5L-SB-DBTCI are presented in order from top to bottom: (a) Input voltage Vin, (b) DC-link.*

The simulation results for 5L-SB-DBTCI are shown in Fig. 8. Fig 8 depicts the input voltage Vin=100Vdc (a). Figure 8(b) shows the DC-link with a shoot-through ratio of d_{st} = 0.2 and a V_{PN} reaches medium voltage at $173V_{dc}$ behind the impedance network.

Fig 9 illustrates the output voltage, which is much higher than the conventional inverter arrangement. It shows 5 voltage levels exactly as theoretically calculated, the effective value reaches 373 Vrms with d_{st} = 0.2. The root mean square current reaches $8A_{RMS}$ with resistive load 40Ω.

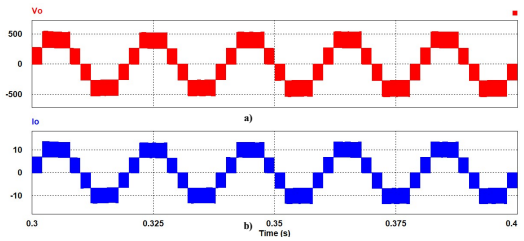

Fig. 9. *(a) Output voltage Vo, (b) Output current Io*

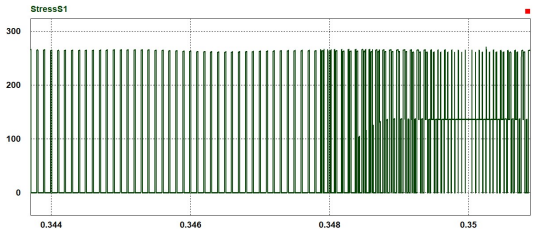

Fig. 10. *Voltage stress on S_1*

Figure 10 shows the stress voltage on S_1. The stress voltage placed on component S_1 (switch with the highest operating frequency in one cycle) reaches 83V.

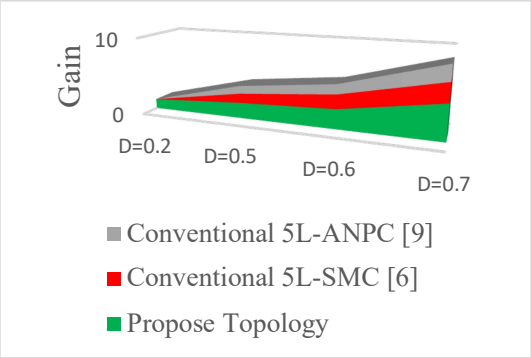

Fig. 11. Compare the voltage gain of the proposed topology with conventional topology.

Figure 11 shows a comparison with traditional topologies, the proposed configuration shows better performance at low d_{st} range. Higher voltage gain but reduces disadvantages such as intermittent input current, voltage stress on large components, etc.

6. CONCLUSION

The 5L-SB-DBTCI topology, which is suitable for PV system with grid connected or EV, has been presented in this paper and is controlled by the PS algorithm. The output voltage results are perfectly as predicted, and the 5L-SB-DBTCI arrangement has higher voltage gain than the other convntional MLI. The output voltage is raised by the introduction of a shoot-through insertion algorithm.

This paper discusses circuit analysis as well as operating theory. PSIM software is used to run the simulation and verify accuracy. The outcomes of simulation and calculation are equivalent.

ACKNOWLEDGMENTS

This work was supported by the Advanced Power Electronics Laboratory D405 of Ho Chi Minh City University of Technology and Education, Viet Nam.

REFERENCES

[1] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano and G. Panda, "Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation," in IEEE Access, vol. 7, pp. 54888-54909, 2019.

[2] A. Poorfakhraei, M. Narimani and A. Emadi, "A Review of Multilevel Inverter Topologies in Electric Vehicles: Current Status and Future Trends," in IEEE Open Journal of Power Electronics, vol. 2, pp. 155-170, 2021.

[3] Bughneda, A., Salem, M., Richelli, A., Ishak, D., & Alatai, S. (2021). Review of Multilevel Inverters for PV Energy System Applications. Energies, 14(6), 1585.

[4] S. K. Kuncham, K. Annamalai and N. Subrahmanyam, "A Two-Stage T-Type Hybrid Five-Level Transformerless Inverter for PV Applications," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9510-9521, Sept. 2020.

[5] Sivasubramanian, M., & Boopathi, C. S. (2021). A Switched Capacitor Based Seven Level Active Neutral Point Clamped (ANPC) Inverter Topology with Reduced Switching Devices. Journal of Electrical Engineering & Technology

[6] J. Yu, R. Burgos, Q. Wang and I. Agirman, "Design of a SiC-based Five-Level Stacked Multicell Converter for High-Speed Motor Drives," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 4063-4068.

[7] Quach, T.-H., Do, D.-T., & Nguyen, M.-K. (2019). A PWM Scheme for Five-Level H-Bridge T-Type Inverter with Switching Loss Reduction. Electronics, 8(6), 702.

[8] X. Zhu et al., "Leakage Current Suppression of Single-Phase Five-Level Inverter for Transformerless Photovoltaic System," in IEEE Transactions on Industrial Electronics, vol. 68, no. 11, pp. 10422-10435, Nov. 2021

[9] Y. P. Siwakoti, "A new six-switch five-level boost-active neutral point clamped (5L-Boost-ANPC) inverter," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 2424-2430,

[10] D. -T. Do and M. -K. Nguyen, "Three-Level Quasi-Switched Boost T-Type Inverter: Analysis, PWM Control, and Verification," in IEEE Transactions on Industrial Electronics, vol. 65, no. 10, pp. 8320-8329, Oct. 2018

[11] S. S. Lee and K. -B. Lee, "Switched-Capacitor-Based Modular T-Type Inverter," in IEEE Transactions on Industrial Electronics, vol. 68, no. 7, pp. 5725-5732, July 2021

[12] V. T. Tran, M. K. Nguyen, D. T. Do, D. Vinnikov, “An SVM scheme for three-level quasi-switched boost T-type inverter with enhanced voltage gain and capacitor voltage balance,” IEEE Trans. Power Electron., vol. 36, no. 10, pp. 11499 - 11508, Oct. 2021.