DIGITAL PI CONTROLLER DESIGN FOR NON-IDEAL LOAD-RESISTOR SYNCHRONOUS BUCK CONVERTER

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ABSTRACT

In this paper, a Continuous Proportional Integral controller is designed for the DC-DC Synchronous Buck Converter, which provides stable average output voltage and inductor current against load or setpoint changes. The control method relies on Average Current Mode Control, tuning the parameters in the frequency domain using a step-wise Loop Shaping process before discretizing the controller. For accurate control, the non-idealities of the Synchronous Buck Converter have been included in its mathematical model. All inherated time delays caused by Analog/Digital conversion, computation, Zero-OderHold and Pulse-Width-Modulation are also considered. Finally, the software tool PSIM is used to obtain the simulation result of the controller.

Keywords: *Synchronous Buck Converter, Mathematical Modelling, Digital Controller, Proportional Integral controller, Loop Shaping, Average Current Mode Control.*

1. INTRODUCTION

Over the last few decades, the DC-DC power converters, which have the objective of providing a DC output voltage, have undergone rapid development [1]. Additionally, as battery technology advances, the number of Electric Vehicles and portable devices is constantly rising. DC voltage appears to be the future's fashion. It's been used in a wide range of industrial applications, such as renewable energy processing, battery charging, personal computers, etc [2]. Therefore, high-quality, trustworthy, flexible, and efficient DC voltage conversion is crucial. Among DC-DC converters, the Buck and Synchronous Buck Converter is used whenever there is a need to lower the input DC voltage. Usually, the Synchronous Buck Converter offers higher efficiency than the asynchronous one [3]. However, it is challenging to achieve a constant output voltage at a constant duty cycle in open-loop DC-DC converters due to variations in input voltages, output loads, and the nonlinear properties of circuit elements.

Therefore, a feedback loop is needed. For duty cycle control, classical linear feedback is most frequently utilized. The mathematical modeling of the converters is required in designing a proper control scheme, and the parasitic components should be included in the model's design for optimal control. In this paper, it is discussed in Section II.

Further, the inherent problems when using digital controllers will be discussed. As shown in Fig. 1, where T_s is the sampling period of the sampler, a digital structure will add 4 new factors that are inherent to any digital control system, impacting the stability and internal gains of the control loop that are not included in a conventional analog feedback control system: the A/D and D/A restricted resolutions, the computational time, a ZOH for the holding effect of the DAC and an Anti-Aliasing Filter. However, due to the misconception that they have a negligible impact on the system, many researchers frequently overlook them. For precise control, their impact must be taken into account while designing the control loop. Then, the system will lose phase, causing bandwidth limitations and design challenges. The delay makes its phase further lag as the frequency increases, again distorting the phase response and violating the Bode law [6]. The simple approach outlined in many theoretical books for the Bode plot will not be successful in predicting instability in these particular circumstances. An alternative method is to directly influence the loop's Bode plot. In this paper, Loop Shaping approach for PI controller tuning will be discussed in section III. The s-domain controller is then digitized in order to obtain a difference equation, which can be directly programmed. Section IV presents the simulation and experimental results, followed by the conclusion in section V and references.

2. LOOP GAIN TRANSFER FUNCTION

2.1. Mathematical Model Of Non-Ideal DC-DC Converter

The basic topology of a Non-ideal DC-DC Synchronous Buck Converter is shown in Fig. 2. It consists of 2 MOSFETs Q_1 and Q_2, with an L-C filter. V_{in} is the input DC voltage source, and V_o is the output DC voltage across the load resistance. For precise modeling of Synchronous Buck Converter, the different non-idealities such as the Equivalent Series Resistance (ESR) of the inductor r_L, the ESR of the capacitor r_C, and the static Drain-Source on resistance of 2 MOSFETs r_{sw1} and r_{sw2} have been considered. The converter is assumed to operate in Continuous Conduction Mode (CCM) with duty cycle D and switching frequency f. There will be 2 main switching modes in the converter:

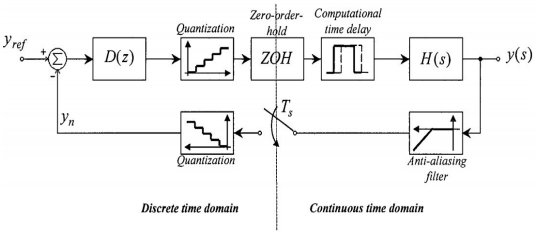

Fig. 1. *The digital equivalent of an analog control loop [5]*

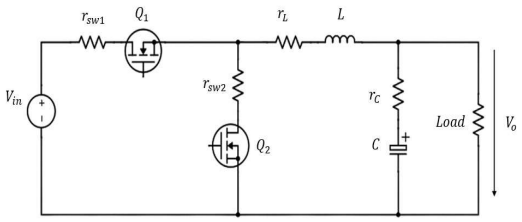

Fig. 2. *Non-ideal Synchronous Buck Converter configuration*

1) Q_1 *is ON and* Q_2 *is OFF:*

$$\begin{cases} L\dfrac{di_L(t)}{dt} = v_{in}(t) - v_o(t) - (r_{sw1} + r_L)i_L(t) \\ C\dfrac{dv_C(t)}{dt} = i_L(t) - \dfrac{v_o(t)}{R} \\ v_o(t) = v_C(t) + r_C C\dfrac{dv_C(t)}{dt} \end{cases} \quad (1)$$

2) Q_1 *is OFF and* Q_2 *is ON:*

$$\begin{cases} L\dfrac{di_L(t)}{dt} = -v_o(t) - (r_{sw2} + r_L)i_L(t) \\ C\dfrac{dv_C(t)}{dt} = i_L(t) - \dfrac{v_o(t)}{R} \\ v_o(t) = v_C(t) + r_C C\dfrac{dv_C(t)}{dt} \end{cases} \quad (2)$$

Here, $i_L(t)$, $v_c(t)$, $v_{in}(t)$ and $v_o(t)$ are instantaneous values of inductor current, capacitor voltage, input voltage and output voltage, respectively.

To derive the mathematical model of the converter, the State-Space Averaging (SSA) technique has been used [7]. Equations from (1) and (2) are averaged throughout one switching period with corresponding duty cycles as weights. Then, by introducing small pertubations around the DC operating point, the small-signal linearized model is obtained. The transfer function model is then obtained using the Laplace transform, with the input voltage is assumed to be constant. The duty cycle to inductor current small-signal transfer function and the inductor current to output voltage small-signal transfer function have been obtained as:

$$G_{id}(s) = k_1 \cdot \frac{s + b_{01}}{s^2 + a_{11}s + a_{01}} \quad (3)$$

With

$$\begin{cases} k_1 = \dfrac{V_{in}}{L} \\ b_{01} = \dfrac{1}{(R + r_C)C} \\ a_{11} = \dfrac{L + C[(Dr_{sw1} + r_L + (1-D)r_{sw2})(R + r_C) + Rr_C]}{(R + r_C)CL} \\ a_{01} = \dfrac{Dr_{sw1} + r_L + (1-D)r_{sw2} + R}{(R + r_C)CL} \end{cases}$$

$$G_{vi}(s) = k_2 \cdot \frac{s + b_{02}}{s + a_{02}} \quad (4)$$

With

$$\begin{cases} k_2 = \dfrac{Rr_C}{(R + r_C)C} \\ b_{02} = \dfrac{1}{Cr_C} \\ a_{02} = \dfrac{1}{(R + r_C)C} \end{cases}$$

2.2. Anti-Aliasing Filter

Whenever a measured analog signal is sent to a digital control structure, an Analog-to-Digital Converter (ADC) is required to carry out the discretization and quantization of the signal coming in. In noisy applications, a powerful additional low-pass filter is needed to dampen the analog high frequencies so that the frequency folding (aliasing) phenomenon inherent to any sampled system is avoided. For Switched Mode

Power Supplies, where the sampling frequency is much higher than the highest dynamic of the process, the Anti-Aliasing filter can be reduced to a high frequency low-pass filter with a high cut-off frequency whose influence on the stability of the open loop system can be neglected in the frequency range of the cross-over frequency of the controller [5]. A RC low-pass filter is characterized by the cutoff frequency ω_0, which can be calculated as $\frac{1}{RC}$. Thus, the following Laplace transfer function is:

$$G_{LPF}(s) = \frac{1}{\frac{s}{\omega_0} + 1} \tag{5}$$

The cutoff frequency should be selected to be higher than the Nyquist Frequency, while being sufficiently enough to avoid phase lag at the closed-loop system's bandwidth frequency.

2.3. Computation Delay

Once the A/D conversion is completed, the control algorithm processes the quantified output value to choose the appropriate control action. Due to the microprocessor's restricted operating frequency and the A/D-D/A conversion time, there will be a delay between the time the process output is sampled and when the control variable is updated. The simpler method entails updating the control variable as soon as the computations are finished. Thus, the delay depends on the CPU frequency clock, the A/D-D/A sampling rate and the conversion time, and can be shortened or lengthened due to some software glitches. In Switched Mode Power Supplies, updating the control variable immediately might even cause serious problems during large transients since the switch's gating can be triggered twice within one switching cycle. [5] suggests an alternative option is to update the control variable only at the beginning of the subsequent sampling period, thus ensuring a fixed delay of a sampling period (T_s), which is only slightly longer than the delay introduced in the straightforward implementation.

2.4. Sample & Hold

A Zero-Order-Hold is used to bridge the gap between a discrete signal and its continuous equivalent. It reconstructs the continuous signal based on a train of pulses by holding its input for the duration of a sampling cycle. The effect of the hold circuit can be represented by a pure delay of half of the sampling period ($T_s/2$). Actually, the approximation is only accurate in phase, but the error in gain is sufficiently negligible to be disregarded. The ADC also has the effect of holding the measured signal during the whole sampling time. However, the controlled system is only impacted by the ADC conversion time, which is very small. The way the microcontroller's registers and buffers store data for processing functions similarly.

2.5. Modulation Delay

In Switched Mode Power Supplies, some time will have elapsed between the instant a new duty cycle is updated in the modulator and the instant that duty cycle is reflected into a pulse. For saw-tooth carrier, the delay is DT_{sw} and for inverted saw-tooth carrier, the delay is $(1-D)T_{sw}$. For controller tuning, the average value is often utilized for both saw-tooth carrier shapes. With a triangular carrier, both the rising and falling edges of the PWM signal are affected by the duty cycle value. A small-signal approximation introduced in [8] and further developed in [9] shows that the delay is $\frac{T_{sw}}{2}$.

2.6. Discussion

The description above shows that inherent elements such as Zero-Order-Hold and computational time delay must be considered in the controller desired. Otherwise, the stability of the entire system can degrade seriously. As a result, the bandwidth of the closed-loop system will have to be reduced in comparison to a pure analog control design. These delays are highly influenced by the sampling period. Thus, they can be minimized by using higher rating components and oversampling ($T_s < T_{sw}$). However, according to [9], oversampling can result in other problems akin to aliasing, and require another Digital Anti-Aliasing Filter.

The sampling frequency for digital control systems is chosen according to the desired bandwidth of the closed-loop system. As a rule of thumb, the sampling frequency is set from about 6 to 25 times the closed-loop system bandwidth frequency [10]. According to [5], the best choice is to take $T_s = T_{sw}$. Then, the total delay is $2T_s$:

$$Gdelay(s) = e^{-2sTs} \tag{6}$$

Now the Current Loop Gain transfer function can be described as follows:

$$Gcur(s) = GLPF(s) \cdot Gid(s) \cdot Gdelay(s) \tag{7}$$

3. CONTROLLER DESIGN

3.1. Problem Formulation

The block diagram in the s-domain for the closed-loop. Current Mode Control of the Non-ideal Synchronous Buck Converter is shown in Fig. 3. It contains 2 cascaded control loops: an internal current control and an external voltage control loop for improvement. The actual output voltage (v_o) is compared with the desired output voltage ($v_{o,ref}$). The controller ($G_{PI,vol}$) would process the error to generate input for the inner current loop ($i_{L,ref}$). The inner current loop will follow the same approach, with the measured signal being the real inductor current (i_L) and the output signal being the duty cycle (d). This control signal is compared with a fixedfrequency saw-tooth waveform to

produce the switching pulses of the required pulse width. For the Digital PWM Modulator, the Lapace transfer function can be represented as 1.

The parameters of the Non-ideal Synchronous Buck Converter under examination are given in Table I. Substituting these values in (3) and (4), the transfer functions of the converter can be obtained as:

$$G_{id}(s) = \frac{9.137 \cdot 10^4 \cdot s + 2.501 \cdot 10^7}{s^2 + 1335s + 1.398 \cdot 10^7} \quad (8)$$

$$G_{vi}(s) = \frac{0.2956s + 5473}{s + 273.7} \quad (9)$$

As previously indicated, $T_s = T_{sw} = \frac{1}{f} = 20 \cdot 10^{-6}$ s. Thus, the delay transfer function is: $-40 \cdot 10^{-6} \cdot s$

$$G_{delay}(s) = e \quad (10)$$

With a 50kHz sampling frequency, the closed-loop bandwith frequency should be less than 5kHz. A 1000Ω resistor and 10nF capacitor can be used for the RC low-pass filter. As a result, the cutoff frequency is about 15.9kHz and the following transfer function can be calculated as:

$$G_{LPF}(s) = \frac{1}{10^{-5} \cdot s + 1} \quad (11)$$

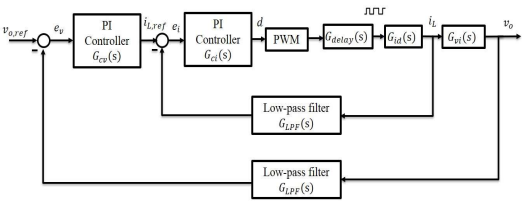

Fig. 3. *Block diagram of the double-loop PI controller for the converter*

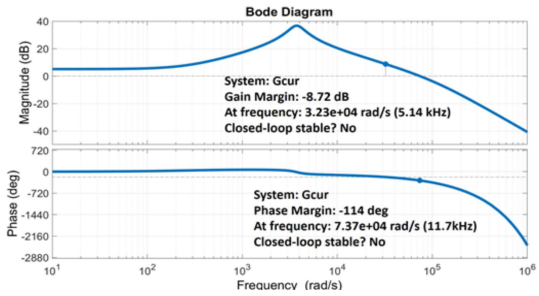

Fig. 4. *Frequency response of the uncompensated current loop*

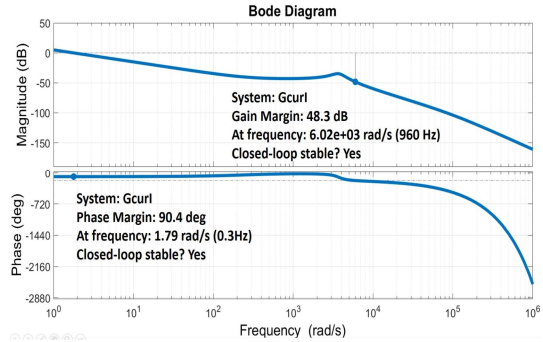

Fig. 5. *Frequency response of the current loop using Integral controller*

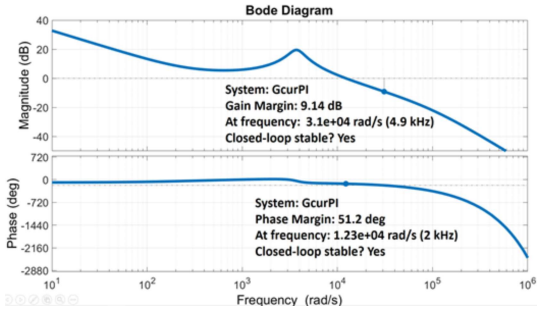

Fig. 6. *Frequency response of the current loop using PI controller*

3.2. Inner Current Loop Controller Design

The Current Loop Gain transfer function can be obtained as follows by combining (7), (8), (10) and (11):

$$G_{cur}(s) = \frac{9.137 \cdot 10^4 \cdot s + 2.501 \cdot 10^7}{(s^2 + 1335s + 1.398 \cdot 10^7)(10^{-5} \cdot s + 1)} \cdot e^{-4 \cdot 10^{-5} \cdot s} \quad (12)$$

The frequency response of the uncompensated current loop is shown in Fig. 4. Via the Bode plot, it is shown that the closed loop is not stable. The Phase

Margin have decreased as a result of the delay components. Additionally, the gain is constant from low frequencies to the frequency of the zero at 274rad/s, which gives steady-state error for any step disturbance in the system. To eliminate the steady-state error, a single pole at the origin can be added.

Table I. The non-ideal synchronous buck converter parameters

Parameter	Symbol	Value	Unit
Input voltage	*Vin*	12	V
Output voltage	*Vo*	4.2	V
Inductor current	*Io*	0.9	A
Load resistance	*R*	20	Ω
Switching frequency	*f*	50	kHz
Inductance	*L*	394	μH
ESR of the inductor	*rL*	0.12	Ω
Capacitance	*C*	180	μF
ESR of the capacitor	*rC*	0.3	Ω
Static Drain-Source on resistance of Q_1	*rsw*1	0.0026	Ω
Static Drain-Source on resistance of Q_2	*rsw*2	0.0026	Ω

Fig. 5 shows the frequency response of the new plant. The closed loop is stable, but the crossover frequency is very low, even if the gain of the controller increases. Thus, it is required to add another zero at the frequency around the natural frequency (3739rad/s) in order to make the slope after passing the peak increase to −20dB/dec, causing the crossover frequency to become higher and ensuring a stable system. With the added zero *z*, it can be seen that at a specific crossover frequency, the higher *z* increases, the lower the phase is. The phase also decreases as the crossover frequency increases. After careful consideration in choosing the crossover frequency and the Phase Margin, it was able to add a zero at 2000rad/s. Then, by raising the gain factor to 244, the system's Phase Margin can be achieved to 51.2° at the crossover frequency of $1.23 \cdot 10^4$rad/s (1.96kHz), as shown in Fig. 6. It can also be shown that the Gain Margin is 9.14dB at $3.1 \cdot 10^4$rad/s (4.9kHz), which is typically enough. The controller has the transfer function as described in (13). It can also be represented as a Parallel PI controller with $k_P = 0.123$ and $k_I = 244$.

$$G_{ci}(s) = 244 \cdot \frac{1 + 0.0005s}{s} \tag{13}$$

3.3. Outer Voltage Loop Controller Design

In cascade control loops, it is possible to consider the inner current control loop to be fast enough and can be

ignored when designing the controller for the outer voltage loop. However, it is also required to double-check the influence of the inner loop on the outer loop. The Voltage Loop Gain transfer function can be obtained by multiplying (9) by (11):

$$G_{vol}(s) = \frac{0.2956s + 5473}{(s + 273.7)(10^{-5} \cdot s + 1)} \quad (14)$$

The frequency response of the uncompensated current loop is shown in Fig. 7. Via the Bode plot, it is shown that the Gain Margin is infinity, which means no matter how much the gain rises, the system will always be stable. Compared to the inner loop, the system is more straightforward due to the absence of complex conjugate poles. Firstly, add a single pole at the origin to neutralize the steady-state error. The slope of the Loop Gain at the crossover frequency is now −40dB/dec. Add a zero to cancel the effect of the pole at 273.7rad/s and increase the slope at the crossover frequency to −20dB/dec. Now the gain term can be changed to reach the desired crossover frequency. For the crossover frequency of 201rad/s to ensure the internal loop is very fast compared to the external loop, the compensator's gain is 10. Fig. 8 shows that the Phase Margin is now 90.8° at 201rad/s. The closedloop is stable with a Gain Margin of infinity. The controller has the transfer function as described in (15) and can also be represented as a Parallel PI controller with $k_P = 0.037$ and $k_I = 10$.

$$G_{cv}(s) = 10 \cdot \frac{1 + 0.0037s}{s} \quad (15)$$

3.4. Discrete the controller

According to [5], the z-domain equivalent of the controller can be approximated by substituting the Laplace operator s with a function of the discrete operator z. The common approximation functions are the Backward Euler method and the Bilinear Transformation. Those methods are accurate when the sampling rate is 10 times smaller than the smallest time constant of the compensator. The Matched Pole-Zero is also suggested. In order to reduce the sensitivity of the rounding and quantization effects, in the case of the PI controller, better discrete equivalents are obtained by keeping the proportinal and integral actions separate. In this paper, the Backward Euler method is chosen to discrete the analog controller.

$$G_{PI}(z) = k_P + k_I \frac{zT_s}{z - 1} \quad (16)$$

$$uk = kPek-1 + uIk-1 + kITsek \quad (17)$$

4. SIMULATION RESULTS

In this paper, the tool PSIM is used to simulate the performance of the controller. The digital control algorithm is implemented using the Simplified C Block in PSIM.

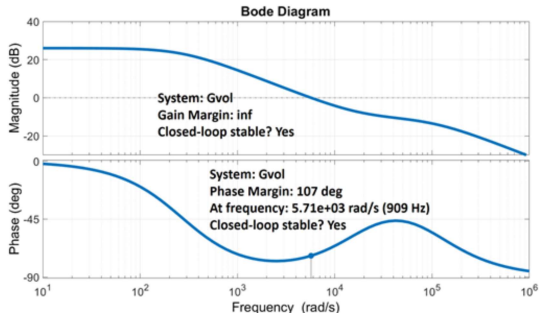

Fig. 7. *Frequency response of the uncompensated voltage loop*

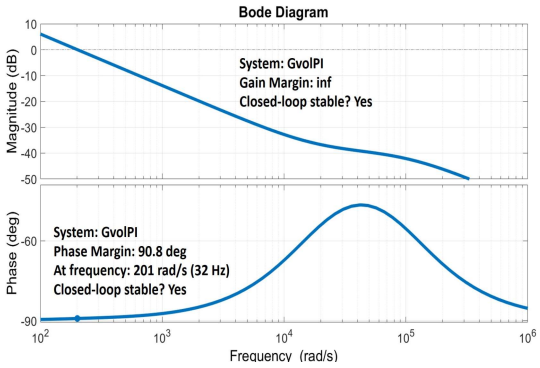

Fig. 8. *Frequency response of the voltage loop using PI controller*

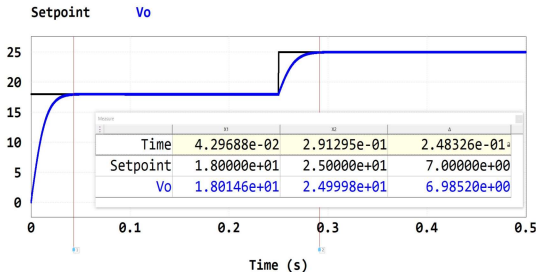

Fig. 9. *The output voltage when the setpoint changes from 18V to 25V*

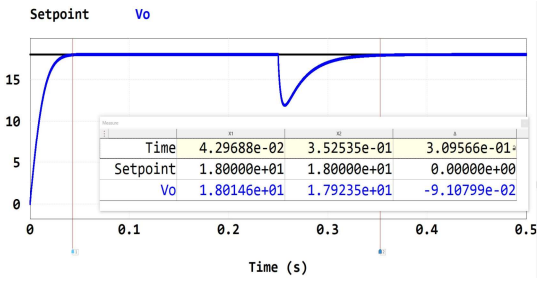

Fig. 10. *The output voltage when the load changes from 20Ω to 10Ω*

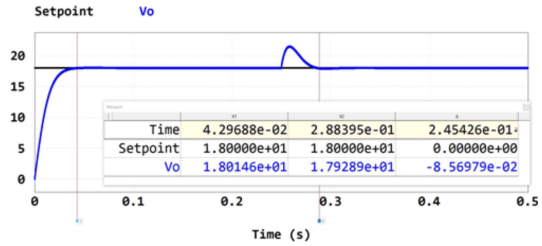

Fig. 11. *The output voltage when the load changes from 20Ω to 30Ω*

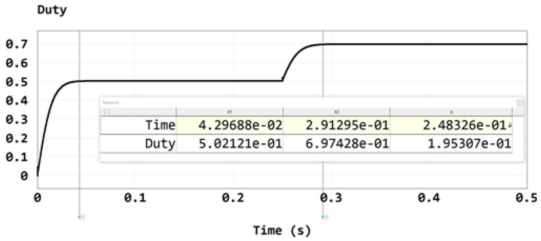

Fig. 12. *The controller output when the setpoint changes from 18V to 25V*

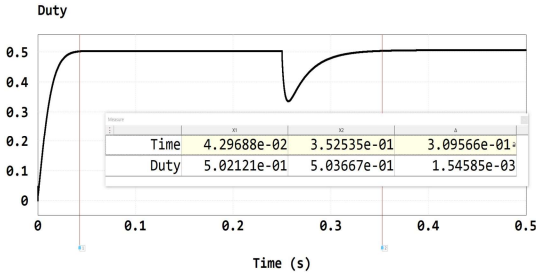

Fig. 13. *The controller output when the load changes from 20Ω to 10Ω*

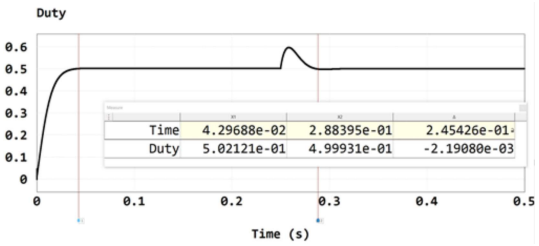

Fig. 14. *The controller output when the load changes from 20Ω to 30Ω*

Fig. 9 shows the performance of the double closed-loop converter for a step variation in the setpoint (from 0V to 18V at 0s and from 18V to 25V at 0.25s) while keeping the load constant at 20Ω. The

desired output voltage tracks the setpoint with no overshoot and no steady-state error within 40ms. The simulation result of the output voltage when the load resistance is varied from 20Ω to 10Ω at 0.25s while keeping the setpoint constant at 18V is shown in Fig. 10. It can be shown that the controller resumes the output voltage to 18V in 100ms. There is no overshoot, and the steady-state error is neutralized thanks to the integral term. Fig. 11 shows the output voltage when the load changes from 20Ω to 30Ω at 0.25s. Due to an undershoot of about 0.3V, transient response time is decreased to 30ms. Fig. 12, Fig. 13 and Fig. 14 show the performance of the controller output in these cases. The controller output performs smoothly. The duty cycle is within the range of 0 to 1 and has not even been driven into saturation. The issue of internal instability doesn't occur.

From the transfer function results when designing the controller, it can be expected that the settling time is about 20ms with no overshoot and no steady-state error. For specific application, due to the output ripple and the switching period, it can be expected that the output voltage will reach the steady state at about 40ms. From the simulation results, it can be shown that the amount of time it takes to reach the steady voltage is about 40ms. However, it becomes 50ms when the load increases and even higher when the load decreases. The discrepancy is due to the converter's own problems, and it also indicates that there is still some impact from the internal current loop on the external voltage loop. It can also proved that the control performance is not really fast due to the limitations on the closed-loop system bandwidth and the tradeoff to avoid overshoot and oscillation. The step and procedure can be used to redesign and get better and faster results, but of course, overshoot and oscillation can occur.

CONCLUSION

In this paper, a digital PI controller based on a continuous time domain approach using the Loop Shaping method is designed for the Non-ideal Synchronous Buck Converter. It has been shows that the inherent delays due to both software and hardware introduce a large phase lag on the closed-loop system, resulting in low control performances. Finally, the performance of the controller has been verified with the simulation results. The controller performs well enough to provide stability with the step change in setpoint and load resistance. The design steps can also be used under examination to get a better response.

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