GATE DRIVER DESIGN FOR SYNCHRONOUS BUCK CONVERTER

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ABSTRACT

The popularity of lithium-ion batteries in various mobility and energy storage applications has driven increasing demand for efficient and reliable battery charging solutions. Synchronous Buck Converters have gained prominence as a viable choice for regulating the charging voltage and current in these applications due to their inherent advantages, such as high efficiency, compact size, and ease of control. To operate a normally-on MOSFET, it is necessary to use a gate drive with the ability to provide bipolar voltage. The paper suggests utilizing the bootstrap driving method for this purpose. A Double Pulse Test circuit is proposed based on Synchronous Buck Converters to analyze and evaluate MOSFET working characteristics at the operating point. Simulation results confirm the operation of the proposed circuit.

Keywords: *MOSFET, gate driver, boostrap, parasitic parameter, DPT.*

1. INTRODUCTION

Over the last few decades, the DC-DC power converters, which have the objective of providing a DC output voltage, have undergone rapid development [1]. Additionally, as battery technology advances, the number of Electric Vehicles and portable devices is constantly rising. DC voltage appears to be the future's fashion. It's been used in a wide range of industrial applications, such as renewable energy processing, battery charging, personal computers, etc [2]. Therefore, high-quality, trustworthy, flexible, and efficient DC voltage conversion is crucial. According to Fang Lin Luo and Hong Ye, more than 800 different topologies currently exist. Boost, Buck, and Buck-Boost are the most widely used DC/DC power converters [3]. Among DC-DC converters, the Buck Converter, sometimes called the "DC to DC Step Down Converter", is used whenever there is a need to lower the input DC voltage. The conventional Buck Converter is great. But due to high switching losses when MOSFET operates at high switching frequencies and losses that come from freewheeling diode, the overall efficiency of

conventional Buck Converter is typically greatly reduced. The Synchronous Buck Converter is an improvement. Usually, the Synchronous Buck Converter offers higher efficiency than the asynchronous one, mainly due to the replacement of the diode by a FET switch, because the FET conduction resistance is small and does not have the forward voltage drop across it like that with diode in the asynchronous topology [4].

The design of gate driver circuits for Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) is a critical component in Synchronous Buck Converter. These circuits play a pivotal role in controlling the switching characteristics of MOSFETs, influencing system efficiency, and overall performance. As the demand for higher power density, efficiency, and reliability in electronic systems continues to grow, the optimization of gate driver circuits has become a prominent research area [5]. The bootstrap gate drive technique can be used when the input voltage levels prevent the use of direct gate drive circuits for high side N-channel MOSFETs. This method will be presented in detail in section II. In order to assess the properties of power switching components like MOSFETs and IGBTs, double-pulse testing is a common technique. These tests allow for the evaluation of the fast recovery diodes (FRDs), which are frequently used in conjunction with IGBTs, as well as the body diode's and tested element's recovery characteristics in addition to switching characteristics of the tested element. The switching process of the MOSFET in the DPT circuit is analyzed in section III, including the influence of parasitic elements. Section IV presents design considerations for gate driver circuits. Simulation and evaluation results are presented in section V, followed by conclusions in section VI and references.

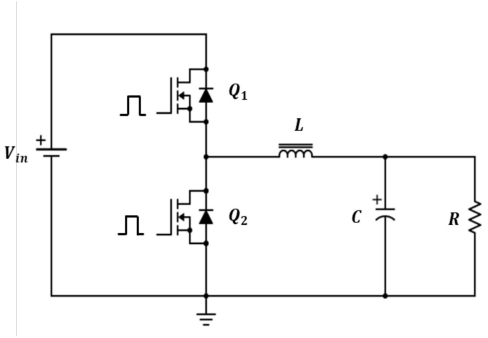

Fig. 11. *Synchronous Buck Converter topology*

2. TOPOLOGY

The bootstrap gate drive approach can be used when the input voltage levels prevent the usage of direct gate drive circuits for high side N-channel MOSFETs. This technique makes use of a gate drive circuit and related bias circuit that are both connected to the source of the primary MOSFET transistor. Along with the device source, the driver and bias circuit oscillate between the two input voltage rails. Nonetheless, since the input voltage is never applied across its components, low voltage circuit parts can implement the

driver and its floating bias. A level shift circuit connects the driver to the ground referenced control signal. This circuit must withstand the significant voltage differential and capacitive switching currents between the ground referenced low side and floating high side circuits.

A typical implementation representing the bootstrap principle is displayed in Fig. ***12***.

V_{in} is the input voltage, V_o is the output voltage. PWM_HS and PWM_LS is the control signal for the highside MOSFET Q_1 anh lowside MOSFET Q_2.

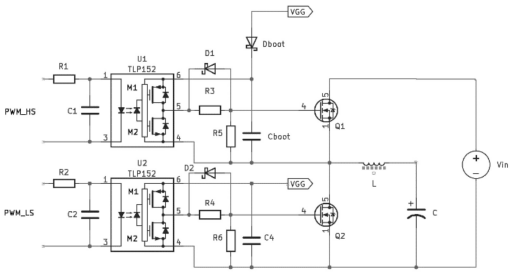

Fig. 12. *Integrated bootstrap driver*

U1 U2 are optocouplers that operate by when there is an input current signal, the LED will light up and MOSFET M_1 is ON, then the output voltage at pin 5 will be equal to the input voltage supplied to it at pin 6.

A boostrap capacitor C_{boost} is used to provide the supply for the highside driver, this capacitor is charged through the diode D_{boost}. The operation of the boostrap circuit is described in the Fig. ***13*** and Fig. ***14***.

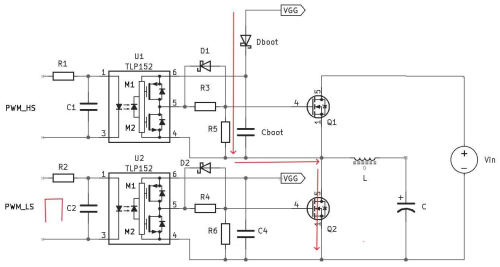

Fig. 13. *MOSFET Q_2 is ON, boostrap capacitor is charged.*

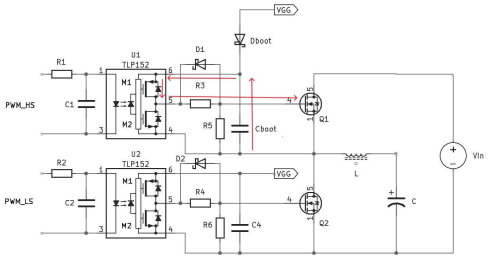

Fig. 14. *MOSFET Q_2 is ON, boostrap capacitor is discharged.*

To test the working characteristics of the MOSFET to properly adjust the gate driver circuit while reducing the risk of current/voltage spikes leading to damage to circuit elements, a Double Pulse Testing (DPT) is used based on Synchronous Buck Converter by short-circuiting the input positive voltage with the output positive voltage [7].

3. SWITCHING INTERVALS ANALYSIS

In this section, the switching process of the MOSFET will be studied stage by stage. The equivalent circuit model considering all the crucial parasitic elements is shown in Fig. ***15***.

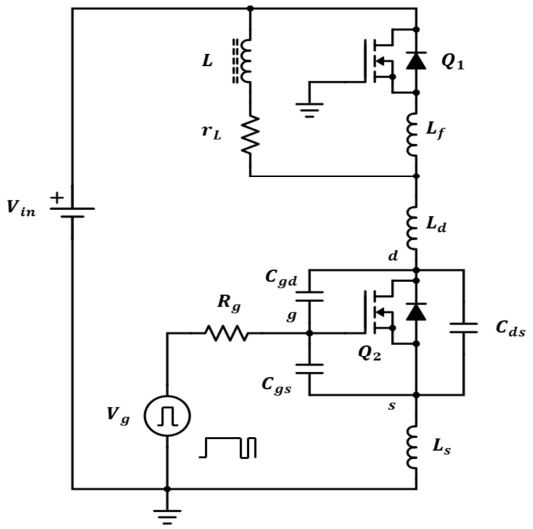

Fig. 15. *Equivalent model of testing circuit with parasitic parameters*

3.1 Analysis the turn-on stage of MOSFET considering parasitic components

The switching waveforms of SiC MOSFET turn-on process can be divided into five stages, as shown in Fig. ***16***.

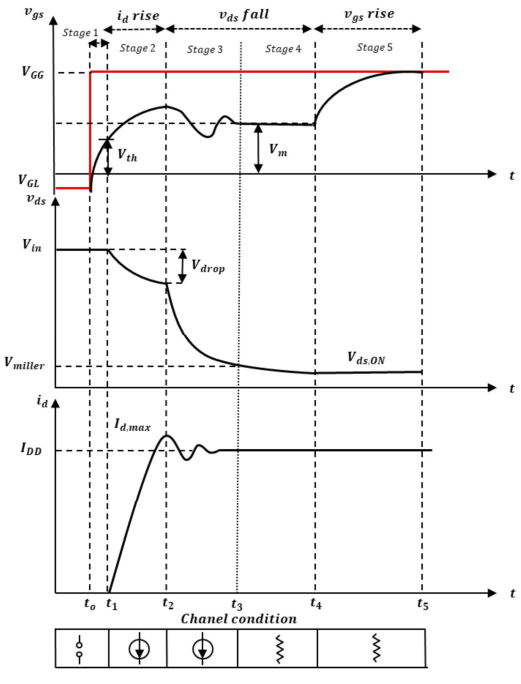

Fig. 16. *MOSFET switching waveform during turn-on process.*

Stage 1 [$t_o - t_1$] turn on delay time: When V_{GG} is used to activate the gate signal and is sent through the resistor R_g, it results in the charging of C_{iss}. During this time neither the V_{ds} voltage nor the I_{ds} current has changed. V_{gs} is given by [6]:

$$v_{gs}(t) = V_{GG}[1 - e^{-\frac{(t-t_0)}{\tau_{iss}}}] \quad (1)$$

Where $\tau_{iss} = R_G(C_{gs} + C_{gd})$.

Stage 2 [$t_1 - t_2$] current rise time: During this stage, the voltage V_{gs} surpasses the threshold V_{th} and the drain current I_{ds} to begin rising from zero to its maximum value, $I_{d,max}$. This peak current is higher than the load current I_{dd} and is generated by the reverse current of the freewheeling diode. The increase in current I_{ds} leads to a decrease in voltage V_{ds} caused by parasitic inductances L_d and L_s:

$$V_{ds,drop} = (L_d + L_s)\frac{di_d}{dt} \quad (2)$$

□2□

However, the relatively stable voltage drops across V_{ds} at this phase enables the presumption that the current passing through the parasitic output capacitances C_{ds} and C_{gd} is minimal when compared to the drain current. Therefore, in the saturation region, the drain current can be represented as:

$$i_d(t) = g_{FS}(V_{gs}(t) - V_{th}) \quad (3)$$

where g_{FS} is the transconductance of SiC MOSFET which is a function of both V_{gs} and V_{ds}.

In this time frame, the circuit equations can be formulated as:

$$V_{GG} = v_{gs}(t) + R_g i_g(t) + L_s \frac{di_d(t)}{dt} \quad (4)$$

$$i_g(t) = \left(C_{gd} + C_{gs}\right) \frac{dV_{gs}(t)}{dt} \quad (5)$$

By combining equations from (2)-(5), $\frac{di_d}{dt}$ is given by:

$$\frac{di_d(t)}{dt} = \frac{g_{FS}(V_{GG} - V_{th}) - i_d(t)}{g_{FS}L_s + R_g C_{iss}} \quad (6)$$

After the drain current $i_d(t)$ reaches the value of I_{DD}, the diode current will reverse its direction and initiate the reverse recovery process. Despite the absence of nonreverse recovery charge in a silicon carbide (SiC) diode, its junction capacitance can still introduce reverse current [6]. The reverse recovery time (t_{rr}) is separated into two segments: t_{rr_1}, when it rises from 0 to $I_{rr,max}$, and t_{rr_2}, when it returns to 0. Reverse recovery time t_{rr} and the maximum reverse current $I_{rr,max}$ are:

$$t_{rr} = \sqrt{\frac{2Q_{rr}(S+1)}{\frac{di_d(t)}{dt}\Big|_{i_d = I_{dd}}}} \quad (7)$$

$$I_{rr,max} = \sqrt{\frac{2Q_{rr}\frac{di_d(t)}{dt}\Big|_{i_d = I_{dd}}}{(S+1)}} \quad (8)$$

□8□

Where Q_{rr} is the reverse recovery charge, S is the snappiness factor which has the value equal to the ratio of t_{rr_2}/t_{rr_1} and $\frac{di_d(t)}{dt}\Big|_{i_d = I_{dd}}$ is the is the current slew rate of i_d at $i_d = I_{dd}$. The peak value of the drain current:

$$I_{d,max} = I_{DD} + I_{rr,max} \quad (9)$$

Stage 3 [$t_2 - t_3$] voltage fall time I: During this stage, the drain current I_d begins to decrease from its peak value, along with the V_{ds} continuing to decrease in the saturation region until it reaches the boundary V_{miller}.

$$V_{miller} = \frac{I_{DD}}{g_{FS}} + V_{th} \quad (10)$$

$$\frac{dv_{ds}}{dt} = \frac{V_{GG} - V_{miller}}{R_g C_{gd}} \quad (11)$$

Stage 4 [$t_3 - t_4$] voltage fall time II: When V_{ds} attains the threshold voltage Vmiller, the MOSFET will transition into the ohmic region. At the completion of this phase, v_{ds} will reach its on-state value, $V_{ds,ON}$.

Stage 5 [$t_4 - t_5$] on-state operation: After v_{ds} reaches $V_{ds,ON}$, it stays at $V_{ds,ON}$, and i_d remains constant at I_{DD}. It is no longer influenced by v_{gs}. Meanwhile, v_{gs} continues to rise and will reach V_{GG} at t_5.

3.2. Analysis the turn-off process of MOSFET considering parasitic components

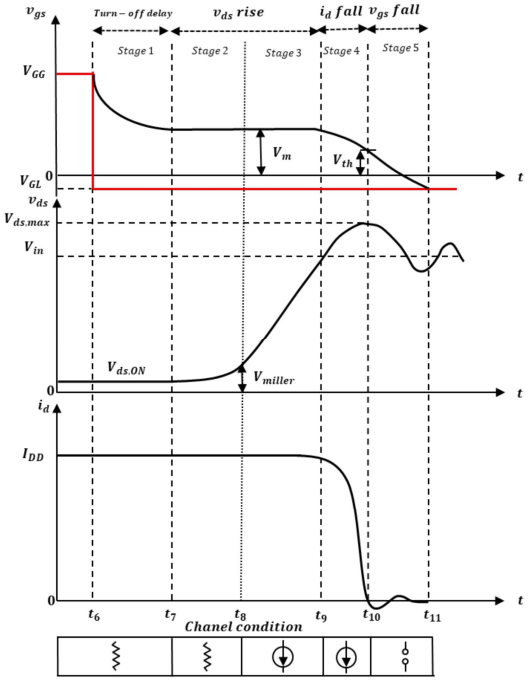

Fig. 17. *MOSFET switching waveform during turn-off process.*

Stage 1 [$t_6 - t_7$] turn off delay time: When the gate drive voltage steps from V_{GG} to 0 at t_6, C_{iss} is discharged through R_g while v_{ds} and i_d remain constant at $V_{ds,ON}$ and I_{dd}.

Stage 2 [$t_7 - t_8$] voltage rise time I: During this period, the MOSFET still works in ohmic region, i_d stays constant at I_{DD} and v_{gs} remain at its Miller voltage. v_{ds} increases to v_{miller} at the end of the stage and the MOSFET begins to enter the saturation region.

Stage 3 [$t_8 - t_9$] voltage rise time II: In this stage, the MOSFET operates in the saturation region as v_{ds} climbs to reach V_{in}. The drain current remains constant, so there is a plateau region in v_{gs} which is also constant.

Stage 4 [$t_9 - t_{10}$] current falling time: At t_9, the FWD starts to conduct when v_{ds} reaches V_{in}. During this time, i_d is moved from the MOSFET channel to the FWD. However, the device is still in its saturation region.

By the same analysis as in the turn-on case, the rate of change of i_d can be depicted as:

$$\frac{di_d(t)}{dt} = -\frac{g_{FS}(V_{GL}+V_{th})+i_d(t)}{g_{FS}L_s+R_gC_{iss}} \quad (12)$$

As to the power loop, v_{ds} can be depicted as:

$$v_{ds}(t) = V_{in} - (L_s + L_d + L_f)\frac{di_d(t)}{dt} \quad (13)$$

where V_{fwd} is the FWD on-state voltage drop. Because $di_d(t)/dt < 0$, $v_{ds}(t)$ will surpass V_{in} when the remaining items are all positive. This stage will extend until the drain current becomes zero and v_{gs} reaches V_{th}.

Stage 5 [$t_{10} - t_{11}$] off-state operation: At the conclusion of stage 4, the turn-off process is complete, but the input capacitance will continue to discharge. In the meantime, after i_d reaches zero at t_{10}, v_{ds} will begin to ring due to resonance between the parasitic inductance of the power loop and the parasitic capacitance C_{oss}.

The natural frequency of the power loop is:

$$\omega = \frac{1}{\sqrt{(L_s+L_d+L_f)C_{oss}}} \quad (14)$$

The analysis mentioned above demonstrates how the turn-off switching transients are a reversely symmetrical process of the turn-on switching transients. Following the stage-by-stage determination of the equations for vds and id, the switching loss can be calculated by integrating them in a full switching transient as:

$$P_{sw} = f_{sw} \int v_{ds}(t) i_d \, dt \qquad (15)$$

4. DESIGN CONSIDERATIONS

A synchronous buck converter is designed with the following specification shown in Table *1*.

Table 1. *Synchronous buck converter design parameters*

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	36	V
Output voltage	V_o	18	V
Output current	I_o	2.5	A
Inductance	L	379	µH
Switching frequency	f	50	kHz
Maximum current	I_{max}	2.74	A

4.1. Gate voltage and current

The turn-on voltage V_{GG} and the turn-off voltage V_{GL} must first be identified. Choosing these 2 parameters wisely will reduce the conduction loss caused by the conduction resistance $R_{DS,on}$. Choosing V_{GG} suitably can balance the conduction and switching loss and choosing V_{GL} sensibly lessens the impact of noise and reverse conduction loss. Of course, these 2 parameters should be suitable for the drive voltage of selected MOSFET, recommend by the manufacturer in the datasheet. For AON6276 that be used in this report, V_{GG} is chosen to be 12V and V_{GL} is chosen to be 0V.

4.2. Gate resistance & Driver IC selection

What value of R_G to choose is one of the most important design decisions that the gate drive designer must make. The switching losses will be reduced by setting R_G to the minimum value; however, dv/dt and EMI will also rise. To make the design as efficient as possible, the designer must research the tradeoffs between switching losses and EMI. Therefore, the selection of resistor R_G can be based on experience, choosing a value for the driving circuit to operate normally and then adjusting and changing the R_G value to achieve the desired results. In this report, the R_G value of 1.5 Ω is chosen to perform simulation and evaluation.

Choose IC TLP152 from TOSHIBA with internal structure as shown in Fig. ***18***. The TLP152 is a photocoupler in an SO6 package that consists of an infrared light-emitting

diode (LED) optically coupled to an integrated high-gain, high-speed photodetector IC chip. The photodetector IC chip has an internal shield to provide a high common-mode transient immunity of ±20 kV/ µs and thus superior noise immunity between the input and output pins. The TLP152 has a totem-pole output that can both sink and source current. It is suitable for directly driving a small IGBT or power MOSFET.

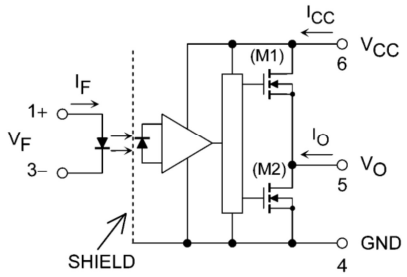

Fig. 18. *TLP 152 internal circuit*

5. RESULT

5.1. Simulation result

Simulation results are used to verify designed parameters. This section reveals the simulation results of DPT circuit using LTSpice. Perform a Double Pulse Test based on the Synchronous Buck Converter circuit. The inductor L has a value of 379 μH to increase the current to the test point during the time of the first pulse $\tau_1 = 29\mu s$, the period for the pulse break τ_{break} and the second pulse τ_2 is selected as $1\mu s$. The double pulse pattern and the current through the inductor are shown in Fig. ***19***. To evaluate the influence of parasitic inductances, choose $L_d = 2\ nH, L_s = 1\ nH, L_f = 0\ nH$ to perform the simulation.

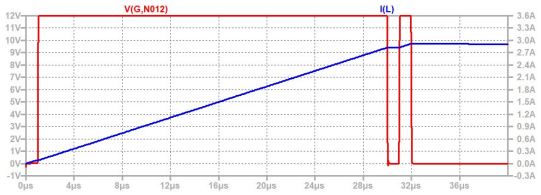

Fig. 19. *Voltage waveform v_{gs} (red) and current load (L) I_{load} (blue)*

The original parameter setup of the waveform calculation is given in Table 2. The variations in the parameters under examination are designed within reasonable ranges of actual conditions.

Table 2. *Setup parameter*

Parameter	Symbol	Value	Unit
Input Capacitor at $v_{ds} = 0V$	$C_{iss@0V}$	5610	pF
Input Capacitor at $v_{ds} = 36V$	$C_{iss@36V}$	4944	pF
Output Capacitor at $v_{ds} = 0V$	$C_{oss@0V}$	4615	pF
Output Capacitor at $v_{ds} = 36V$	$C_{oss@36V}$	862	pF
Forward Transconductance	g_{FS}	100	S
Body Diode Reverse Recovery Charge	Q_{rr}	86	nC
Gate Threshold Voltage	V_{th}	2.6	V

The simulation results of the MOSFET turn-on process are shown in

Fig. **20**. From the simulation results, we obtain the value of the slew rate of the current *di/dt* at I_{DD} is 8190 $(A/\mu s)$. This value is not much different from the calculation result from equation (6): 8658 $(A/\mu s)$. The value of the peak current $I_{d,max}$ calculated from equation (9) is $35.35(A)$, when compared to the simulated value of 29.5A, there is negligible variation. The current waveform and the computation formulae depart from theory, which might be the result of parasitic inductances [8]. In addition, the v_{gs} voltage seems to vary unnaturally; this report makes no mention of this problem.

Next, the simulation results of the turn-off process are depicted in the. According to simulation findings, the value of the $\Delta V_{ds} = V_{ds,max} - V_{in}$ is around 3V, whereas the value derived from equation (13) is 3.2V. In addition, the simulation and calculation's oscillation periods on the vds in stage 5 are 10.34 (ns) and 10.1 (ns) respectively.

Through the comparison of simulation and calculation results, the total parasitic inductances $L_d + L_s$on the experimental circuit can be found. The experimental methods make use of the switching waveform's existing information, which makes them both simple and convincing in presenting the real conditions. The possible methods to find parasitic inductances are:

1. The voltage overshoot at stage 4 of the turn-off process is $\Delta V_{ds} = (L_s + L_d)\,\mathrm{d}i_d(t)/dt$, ΔV_{ds} and $\mathrm{d}i_d(t)/dt$ can be meassured in the turn-off switching waveform, therefore $L_s + L_d$ can be determined.

2. The natural oscillation frequency can be measured using the turn-off switching waveform $\omega = 1/\sqrt{(L_d + L_s)C_{oss@36V}}$, therefore $L_s + L_d$ can be determined.

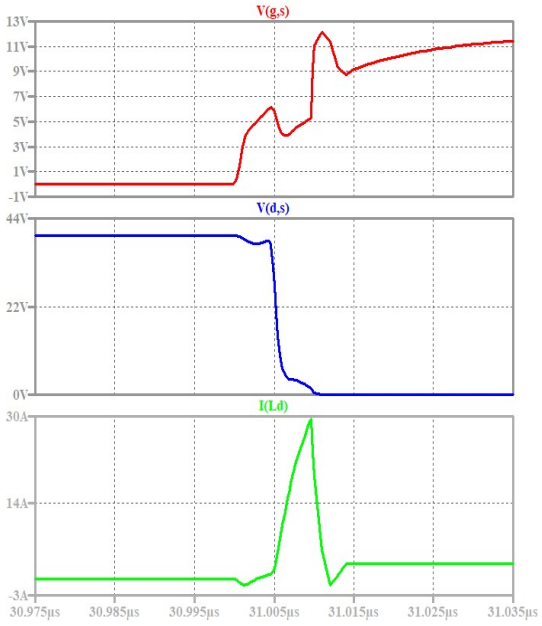

Fig. 20. *Turn-on switching waveform*

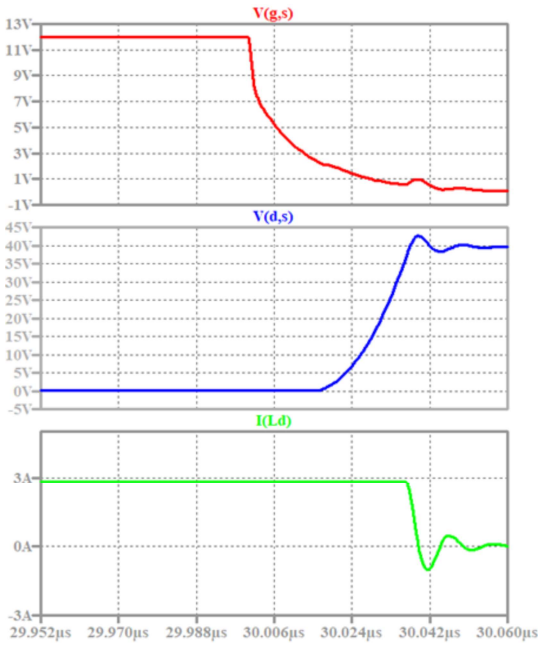

Fig. 21. *Turn-off switching waveform.*

5.2. Effect of R_g

Fig. ***22*** (with turn-on) and **Error! Reference source not found.** (with turn-off) display analytical switching waveforms with varying R_g. It is obvious that with the increase in R_g, the turn-on/turn-off delay of the device will increase beacause the charging/discharging time of the input capacitance increases. The switching speed (both current and voltage slew rates) will generally slow down with big R_g; as a result, spike current and voltage drops that are negatively correlated to the switching speed will all decrease. Furthermore, while the ringing effect on v_{ds} and i_{ds} lowers dramatically when R_g increases, the overshoot voltage ΔV_{ds} during turn-off process will also decrease, but not significantly.

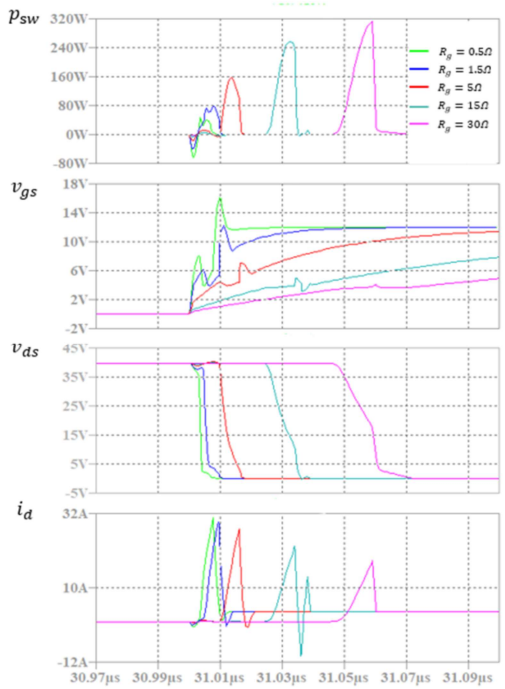

Fig. 22. *Analytical turn-on switching waveform showing the effect of Rg.*

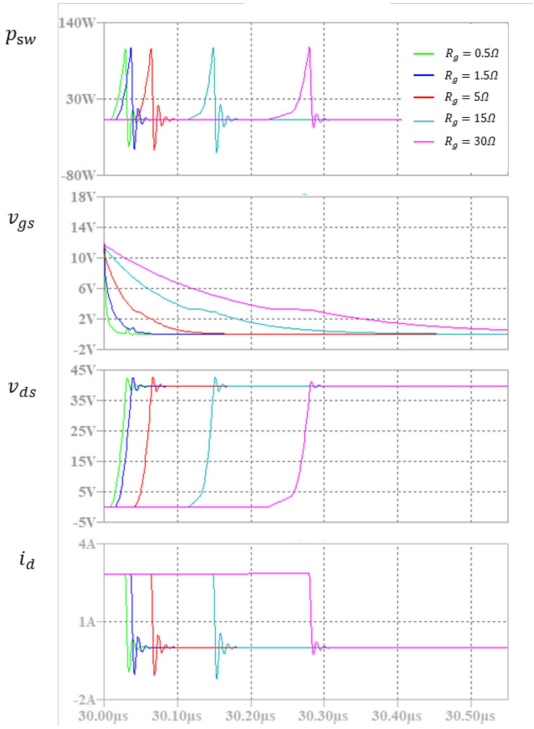

Fig. 23. *Analytical turn-off switching waveform showing the effect of Rg*

Therefore, the value $R_g = 1.5\ (\Omega)$ is perfectly appropriate to balance

switching performance as well as the following impacts when excessive switching speed can harm the MOSFET. To get the best results, it is essential to consider the impact of EMI in the experimental circuit.

CONCLUSION

An investigation on the gate driver design approach used for Synchronous Buck Converters has been done for this paper. In addition, evaluations, and analyses of the phases in the DPT circuit's switching process that involve parasitic components have been described, along with simulations. The article also discusses how switching effects and speed are affected by gate resistance. Nevertheless, additional research is required to assess the impact of additional parasitic elements in trials to optimize switching performance.

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