THE PLANAR TRANSFORMER WINDING LAYOUT METHOD AFFECTS THE PARASITIC CAPACITANCE COMPONENT

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ABSTRACT

The LLC resonant converter is widely used in various high-performance applications. Planar transformers play a crucial role in compact configurations, such as electric bicycle chargers and telecommunications devices, due to their benefits, including low profile, manageable leakage inductance, good thermal characteristics, and ease of production. Designing an LLC resonant converter with a planar transformer poses challenges in minimizing parasitic capacitance from closely spaced coils and managing leakage inductance and winding resistance. Uncontrolled parasitic capacitance can affect the converter's performance. This article delves into parasitic capacitance in planar transformers, highlighting the impact of PCB layout on parasitic capacitance values, simulating validation, and proposing solutions to reduce parasitic capacitance in planar transformers through PCB layout. Conducting experiments with two planar transformers featuring polarized and non-polarized winding structures involves evaluating the quality of parasitic capacitance in these two cases.

Keywords: *LLC converter, Planar transformer, parasitic capacitance.*

1. INTRODUCTION

The LLC resonant transformer is an important type of resonant transformer commonly used in applications like battery chargers for devices such as laptops, phones, and electric vehicles. It benefits from a flanar transformer design due to its compact dimensions and efficient heat dissipation, ideal for space-constrained applications. The high operating frequency of the LLC resonant converter allows the use of printed circuit board (PCB) windings, which reduce copper losses and offer better control over parasitic components like inductance and capacitance compared to round wire windings[1].

However, parasitic components, especially parasitic capacitance, are significant challenges in planar

transformers. Parasitic capacitance includes intra-winding capacitance and inter-winding capacitance, both of which impact the LLC circuit. Inter-winding parasitic capacitance can generate common-mode noise, leading to high EMI noise and affecting resonant current waveforms. Intra-winding parasitic capacitance, modeled as a capacitor across winding ends, increases inrush current, resulting in higher losses[2].

The article explores these issues in-depth, offering detailed modeling and computational techniques for analyzing parasitic capacitance in planar transformers. It also investigates the implications of different PCB layout strategies, supported by extensive simulations and practical experiments[2].

2. MODELING AND CALCULATIONS

2.1. Theory

A capacitor is formed when there is an insulating dielectric material between two conductive objects, and it is referred to as static capacitance in the parasitic capacitance model. The values of capacitance and energy are calculated using the following formulas:

$$C_o = \frac{\varepsilon S}{4k\pi d} \quad (1)$$

$$W = \frac{1}{2} C U^2 \quad (2)$$

In which:

ε: dielectric constant of the material between the two copper layers

S: overlapping area between the two electrodes

d: distance between the two electrodes

k: a constant equal to 9×10^9

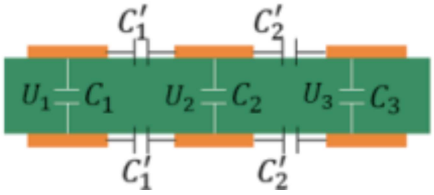

Fig. 1. *PCB with copper serving as a current-carrying conductor*

From the basic knowledge provided and in the context of the research subject of planar transformers (PTs), it is evident that unintended capacitors are formed due to the close proximity of the thin conducting wires carrying electric charge. This formation mainly occurs between consecutive wire layers on the PCB and between adjacent wire loops in a single layer (this part is often neglected due to the thin wire thickness and their close alignment). Show in figure 1.

2.2. Modeling

A fundamental transformer, from an electromagnetic perspective, consists of two ports representing voltages V1 and V2 when there is no electrical connection between its two windings. However, from an electric field viewpoint, an electric field exists between the two windings of the transformer due to the voltage difference between them. This electric field's energy can be analogously represented as a capacitor, thus forming an electrical path between the two windings in the circuit.

In the 6-capacitor model, the transformer operates as a 3-port network, with voltage counterparts V1, V2, and V0 on each port. To facilitate a more comprehensive assessment of the effects of parasitic capacitance, by employing an energy field balance and considering the voltage-current relationships within the planar transformer, we simplify the 6-capacitor model into a single capacitor model connected in parallel with L_m.

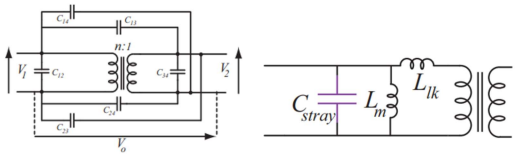

Fig. 2. *a) . Six-capacitor model.*
b) . C_{stray} model

2.3. Calculation

The calculations for parasitic capacitance in a planar transformer can be described as follows.

In the six-capacitor model, we construct the parasitic capacitor model as shown in Figure 1b for two layers connected in series on the PCB, located on the primary and secondary sides, which are different as follows:

$$C_{12} = C_{34} = -\frac{C_0}{6}; C_{13} = C_{24} = \frac{5C_0}{24}; \quad C_{14} = C_{23} = \frac{7C_o}{24} \tag{3}$$

In the scenario where two consecutive wire loops are part of the same winding, the parasitic capacitance model is connected in parallel with these two consecutive loops and is calculated using the following formula:

$$C_{11} = \frac{C_o}{3} \tag{4}$$

When simplifying it to a single parasitic capacitor model, we apply the principle of energy conservation [2].

3. The impact of layout on parasitic capacitance

The issue of parasitic capacitance is a crucial concern primarily stemming from the printed circuit board (PCB) layout. It encompasses a multitude of factors, including the selection of PCB thickness, dielectric materials, copper layer thickness, and the spacing between copper layers. These elements have a profound impact on the static capacitance, denoted as C_0 . Nevertheless, intervening in these factors can be a daunting task, as they are intricately tied to the PCB manufacturing process.

One factor that significantly influences parasitic capacitance and remains open to adjustment is the polarity of the transformer. This aspect of transformer design plays a pivotal role in shaping the overall capacitance characteristics.

In relation to Equation (2), which pertains to the evaluation of parasitic capacitance across the entire winding and for any pair of wire layers within the winding that contribute to parasitic capacitance, it becomes evident that the arrangement and positioning of these wire layers within the winding have a substantial impact on the final value of

parasitic capacitance when it is translated to both the primary and secondary terminals [3]. The intricacies of PCB layout design can further compound this issue. For instance, a choice to connect the polarities of the transformer windings on one side of the PCB can result in an uneven distribution of electric charge between the two windings, ultimately leading to higher parasitic capacitance values when the two polarities are placed opposite each other in the transformer.

In summary, the management of parasitic capacitance in a PCB design is a complex undertaking, involving considerations ranging from material choices and spacing to the inherent polarity of the transformer. Addressing these issues requires a comprehensive understanding of electrical engineering principles and a keen awareness of how the design choices impact the overall performance of the circuit.

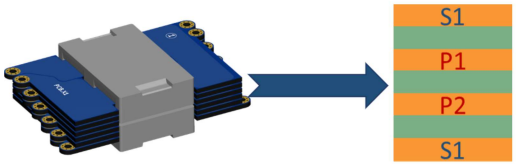

Fig. 3. *A transformer is used to study and the wire structure within a PCB.*

With the transformer depicted in Figure 3, we have the following static parameters:

- The area of the copper layers: $A_t \approx 1638\ mm^2$
- The static capacitance between an outer layer and an inner layer: $C_1 \approx 500\ pF$
- The static capacitance between two inner layers: $C_2 \approx 60\ pF$

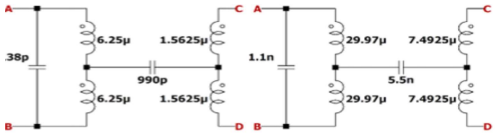

Fig. 4. *The model is split into inter and intra-capacitance, with reversed polarity on the left and unchanged polarity on the right*

The simulation model shown in Figure 4 pertains to two scenarios of transformers with reversed polarities, where the number of wire layers and the wire layer spacing are fixed.

4. EXPERIMENTAL RESULTS

Simulation and experimental data were employed in both scenarios to assess and validate the outcomes. The parasitic capacitance values derived from these simulations and experiments represent the parasitic capacitance values when transformed to the terminals of the wire winding. These values were ascertained by measuring the resonant frequency occurring between C_{stray} and the magnetizing inductance L_m. This resonant frequency measurement is a critical step in evaluating and quantifying

the impact of parasitic capacitance on the system's performance.

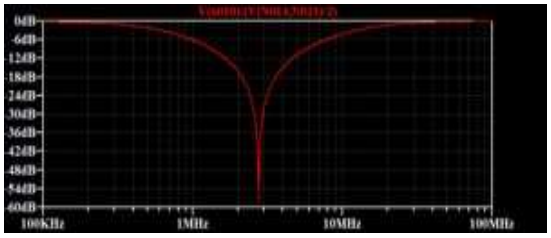

Fig. 5. *Reverse polarity simulation*

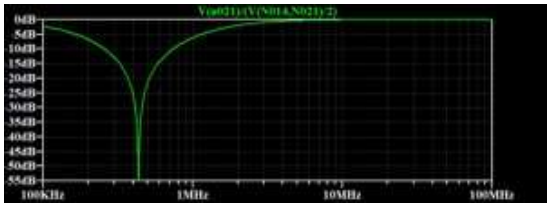

Fig. 6. *Same polarity simulation*

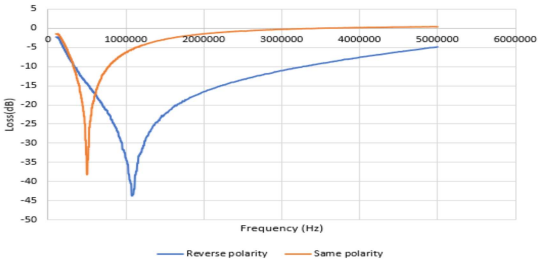

Fig. 7. *Experimental Measurement of Capacitive Reactance*

CONCLUSION

The findings of our research project have not only validated the theoretical framework proposed in the paper but have also revealed an intriguing and practical insight. When comparing the simulation and experimental results for parasitic capacitance (C_stray) in two distinct scenarios, one with polarities in the same direction and the other with polarities reversed, we observed striking differences. The parasitic capacitance was measured at 137.7 pF for the opposite polarity scenario, while it surged to 868 pF for the same polarity setup. This significant sevenfold difference underscores the profound influence of polarity layout on the transformer's parasitic capacitance.

In essence, our study sheds light on the importance of polarity arrangements in transformer design and PCB layouts. It demonstrates that a strategic choice in polarity orientation can drastically reduce unwanted parasitic capacitance. By offering this practical and impactful insight, our research significantly contributes to a deeper understanding of PCB layout techniques that efficiently minimize parasitic capacitance. It also underscores the fundamental theories underpinning this parasitic capacitance phenomenon, thereby advancing our knowledge in the field.

In summary, we began with the fundamental theory of capacitors, elucidating the impact of parasitic capacitance on the LLC circuit. Subsequently, the article delved into how the placement of components on the PCB influences the value of parasitic capacitance. Through evaluation and simulation, we provided readers with an overview and easy control over the parasitic capacitance value in the LLC circuit. This contributes to enhancing the system's performance and stability, offering readers the opportunity to manage and optimize their PCB designs.

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